625kSPS, 24-Bit Analog-to-Digital Converter

FEATURES

- **AC Performance:**
  107dB of Dynamic Range at 625kSPS
  115.5dB of Dynamic Range at 78kSPS
  –115dB THD
- **DC Accuracy:**
  3ppm INL
  2μV/°C Offset Drift
  2ppm/°C Gain Drift
- **Programmable Digital Filter with User-Selectable Path:**
  - **Low-Latency: Completely settles in 5.5μs**
  - **Wide-Bandwidth: 305kHz BW with flat passband**
- **Flexible Read-Only Serial Interface:**
  - **Standard CMOS**
  - **Serialized LVDS**
- **Easy Conversion Control with START Pin**
- **Out-of-Range Detection**
- **Supply: Analog +5V, Digital +3V**
- **Power: 350mW**

APPLICATIONS

- **Automated Test Equipment**
- **Vibration Analysis**
- **Sonar**
- **Test and Measurement**

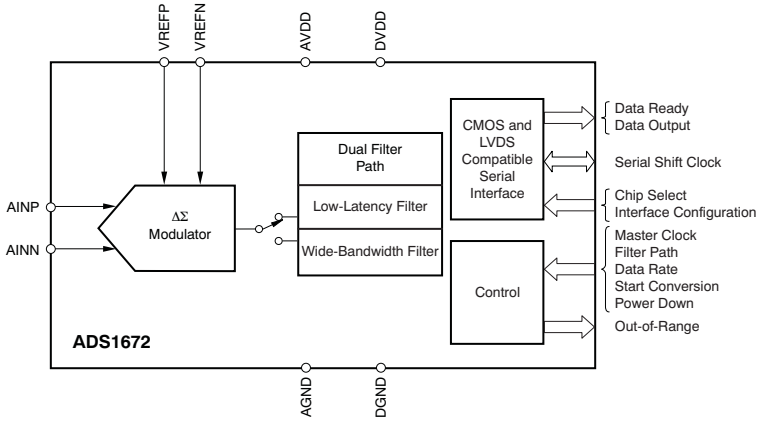
DESCRIPTION

The ADS1672 is a high-speed, high-precision analog-to-digital converter (ADC). Using an advanced delta-sigma (ΔΣ) architecture, it operates at speeds up to 625kSPS with outstanding ac performance and dc accuracy.

The ADS1672 ADC is comprised of a low-drift, chopper-stabilized modulator with out-of-range detection and a dual-path programmable digital filter. The dual filter path allows the user to select between two post-processing filters: low-latency or wide-bandwidth. The low-latency filter settles quickly in one cycle, for applications with large instantaneous changes, such as a multiplexer. The wide-bandwidth path provides an optimized frequency response for ac measurements with a passband ripple of less than 0.001dB, stop band attenuation of 115dB, and a bandwidth of 305kHz.

The ADS1672 is controlled through I/O pins—there are no registers to program. A dedicated START pin allows for direct control of conversions: toggle the START pin to begin a conversion, and then retrieve the output data. The flexible serial interface supports data readback with either standard CMOS and LVDS logic levels, allowing the ADS1672 to directly connect to a wide range of microcontrollers, digital signal processors (DSPs), or field-programmable grid arrays (FPGAs).

The ADS1672 operates from an analog supply of 5V and digital supply of 3V, and dissipates 350mW of power. When not in use, the $\overline{\text{PDWN}}$ pin can be used to power down all device circuitry. The device is fully specified over the industrial temperature range and is offered in a TQFP-64 package.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		ADS1672	UNIT
AVDD to AGND		–0.3 to +6	V
DVDD to DGND		–0.3 to +3.6	V
AGND to DGND		–0.3 to +0.3	V
Input current	Momentary	100	mA
	Continuous	10	mA
Analog I/O to AGND		–0.3 to AVDD +0.3	V
Digital I/O to DGND		–0.3 to DVDD +0.3	V
Maximum junction temperature		+150	°C
Operating temperature range		–40 to +85	°C
Storage temperature range		–60 to +150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTRICAL CHARACTERISTICS

All specifications are at T_A = –40°C to +85°C, AVDD = 5V, DVDD = 3V, f_{CLK} = 20MHz, V_{REF} = +3V, and R_{BIAS} = 7.5kΩ, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADS1672 MIN	ADS1672 TYP	ADS1672 MAX	UNIT
ANALOG INPUTS					
Full-scale input voltage	V_{IN} = (AINP – AINN)		±V_{REF}		V
Common-mode input voltage	V_{CM} = (AINP + AINN)/2		2.5		V
AC PERFORMANCE					
Data rate (f_{DATA})		See Table 2			kSPS
Dynamic range	Inputs shorted together, wide-bandwidth path, f_{DATA} = 625kSPS	105	107		dB
	Inputs shorted together, wide-bandwidth path, f_{DATA} = 78.125kSPS	113	115.5		dB
Signal-to-noise ratio (SNR)	f_{IN} = 10kHz, –0.5dBFS, wide-bandwidth path, f_{DATA} = 625kSPS		102		dB
	f_{IN} = 10kHz, –2dBFS, wide-bandwidth path, f_{DATA} = 625kSPS		103		dB
	f_{IN} = 10kHz, –6dBFS, wide-bandwidth path, f_{DATA} = 625kSPS		99		dB
Total harmonic distortion (THD)	f_{IN} = 10kHz, –0.5dBFS		–105		dB
	f_{IN} = 10kHz, –2dBFS		–109		dB
	f_{IN} = 10kHz, –6dBFS		–116		dB
Spurious-free dynamic range (SFDR)	f_{IN} = 10kHz, –0.5dBFS, signal harmonics excluded		–120		dB
DC PRECISION					
Resolution		24			Bits
Differential nonlinearity			24-bit (monotonic)		
Integral nonlinearity			3	9.5	ppm of FSR
Offset error	T_A = +25°C	–2	1	2	mV
Offset error drift			2		µV/°C
Gain error	T_A = +25°C		1	2	%
Gain error drift			2		ppm/°C
Noise		See Noise Performance table (Table 2)			
Common-mode rejection	At dc		92		dB
Power-supply rejection	At dc, AVDD		92		dB
DIGITAL FILTER CHARACTERISTICS (WIDE-BANDWIDTH PATH)					
Passband		0		0.424f_{DATA}	Hz
Passband ripple				±0.0001	dB
Passband transition	–0.1dB attenuation		0.432f_{DATA}		Hz
	–3.0dB attentuation		0.488f_{DATA}		Hz
Stop band		0.576f_{DATA}		f_{CLK} – 0.576f_{DATA}	Hz
Stop band attenuation			115		dB
Group delay			28		t_{DRDY}
Settling time		See Wide Bandwidth Filter section			
DIGITAL FILTER CHARACTERISTICS (LOW-LATENCY PATH)					
Bandwidth	–3dB attenuation	See Low-Latency Filter section			
Settling time	Complete settling		1		t_{DRDY}
VOLTAGE REFERENCE INPUTS					
Reference input voltage (V_{REF})	V_{REF} = (VREFP – VREFN)	2.75	3.0	3.25	V
VREFP		2.75	3.0	3.25	V
VREFN			Short to AGND		V

ELECTRICAL CHARACTERISTICS (continued)

All specifications are at T_A = –40°C to +85°C, AVDD = 5V, DVDD = 3V, f_{CLK} = 20MHz, V_{REF} = +3V, and R_{BIAS} = 7.5kΩ, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADS1672			UNIT
		MIN	TYP	MAX	
CLOCK (CLK)					
V_{IH}		0.7AVDD		AVDD	V
V_{IL}		AGND		0.3AVDD	V
DIGITAL INPUTS					
V_{IH}		0.7DVDD		DVDD	V
V_{IL}		DGND		0.3DVDD	V
Input leakage	DGND < V_{IN} < DVDD			±10	µA
CMOS OUTPUTS					
V_{OH}	I_{OH} = 2mA	0.8DVDD			V
V_{OL}	I_{OL} = 2mA			0.2DVDD	V
LVDS OUTPUTS					
$\|V_{OD(SS)}\|$	Steady-state differential output voltage magnitude		340		mV
$\Delta\|V_{OD(SS)}\|$	Change in steady-state differential output voltage magnitude between logic states		±50		mV
$V_{OC(SS)}$	Steady-state common-mode voltage output		1.2		V
$\Delta\|V_{OC(SS)}\|$	Change in steady-state common-mode output voltage between logic states		±50		mV
$V_{OC(pp)}$	Peak-to-peak change in common-mode output voltage		50	150	mV
Short-circuit output current (I_{OS})	V_{OY} or V_{OZ} = 0V		3		mA
	V_{OD} = 0V		3		mA
High-impedance output current (I_{OZ})	V_O = 0V or +DVDD		±5		µA
Load				5	pF
POWER-SUPPLY REQUIREMENTS					
AVDD		4.75	5.0	5.25	V
DVDD		2.7	3.0	3.3	V
AVDD current			51	55	mA
DVDD current	CMOS outputs, DVDD = 3V		28	32	mA
	LVDS outputs, DVDD = 3V		33	37	mA
Power dissipation	CMOS outputs, AVDD = 5V, DVDD = 3V		350	370	mW
	Power down		5		mW

DEVICE INFORMATION

TQFP PACKAGE
(TOP VIEW)

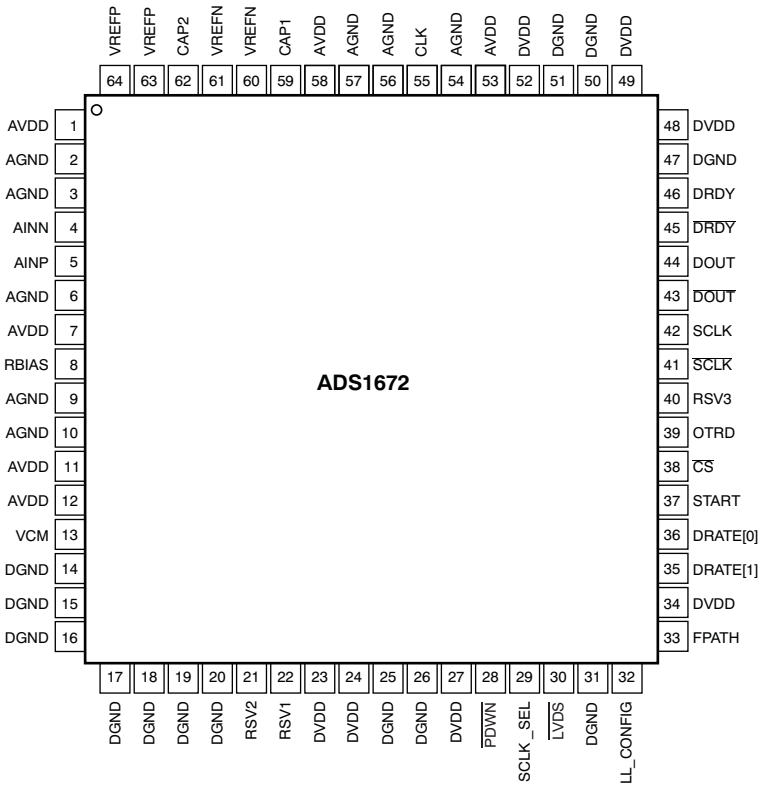


Table 1. TERMINAL FUNCTIONS

PIN		FUNCTION	DESCRIPTION
NAME	NO.		
AVDD	1, 7, 11, 12, 53, 58	Analog	Analog supply
AGND	2, 3, 6, 9, 10, 54, 56, 57	Analog	Analog ground
AINN	4	Analog Input	Negative analog input
AINP	5	Analog Input	Positive analog input
RBIAS	8	Analog	Analog bias setting resistor
VCM	13	Analog	Terminal for external bypass capacitor connection to internal common-mode voltage
DGND	14, 15, 16, 17, 18, 19, 20, 25, 26, 31, 47, 50, 51	Digital	Digital ground
RSV2	21	Reserved	Short to digital ground
RSV1	22	Reserved	Short to digital ground
DVDD	23, 24, 27, 34, 48, 49, 52	Digital	Digital supply
$\overline{\text{PDWN}}$	28	Digital Input	Power-down control, active low
SCLK_SEL	29	Digital Input	Shift-clock source select. If SCLK_SEL = '0', then SCLK is internally generated. If SCLK_SEL = '1', then SCLK must be externally generated.
$\overline{\text{LVDS}}$	30	Digital Input	Serial interface select. If $\overline{\text{LVDS}}$ = '0', then interface is LVDS-compatible. If $\overline{\text{LVDS}}$ = '1', then interface is CMOS-compatible.

Table 1. TERMINAL FUNCTIONS (continued)

PIN		FUNCTION	DESCRIPTION
NAME	NO.		
LL_CONFIG	32	Digital Input	Configure low-latency digital filter. If LL_CONFIG = '0', then single-cycle settling is selected. If LL_CONFIG = '1', then fast-response is selected.
FPATH	33	Digital Input	Digital filter path selection. If FPATH = '0', then path is wide-bandwidth. If FPATH = '1', then path is low-latency.
DRATE[1:0]	35, 36	Digital Input	Data rate selection
START	37	Digital Input	Start convert, reset, and synchronization control input
$\overline{CS}$	38	Digital Input	Chip select; active low.
OTRD	39	Digital Output	Digital filter out-of-range indicator
RSV3	40	Reserved	This pin must be left floating. Do not connect or short to ground.
$\overline{SCLK}$	41	Digital Output	Negative shift clock output. If SCLK_SEL = '0', then $\overline{SCLK}$ is the complementary shift clock output. If SCLK_SEL = '1', then $\overline{SCLK}$ always output is 3-state.
SCLK	42	Digital Input/Output	Positive shift clock output. If SCLK_SEL = '0', then SCLK is an output. If SCLK_SEL = '1', then SCLK is an input.
$\overline{DOUT}$	43	Digital Output	Negative LVDS serial data output
DOUT	44	Digital Output	Positive LVDS serial data output
$\overline{DRDY}$	45	Digital Output	Negative data ready output
DRDY	46	Digital Output	Positive data ready output
CLK	55	Digital Input	Master clock input
CAP1	59	Analog	Terminal for 1µF external bypass capacitor
VREFN	60, 61	Analog	Negative reference voltage. Short to analog ground.
CAP2	62	Analog	Terminal for 1µF external bypass capacitor
VREFP	63, 64	Analog	Positive reference voltage

TIMING CHARACTERISTICS

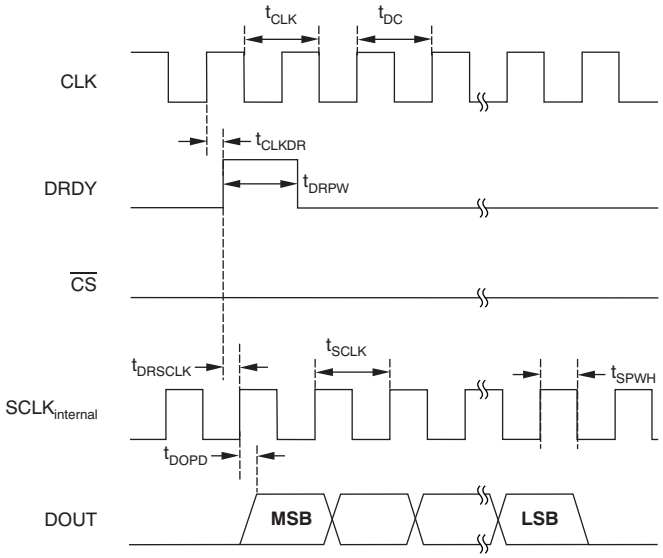
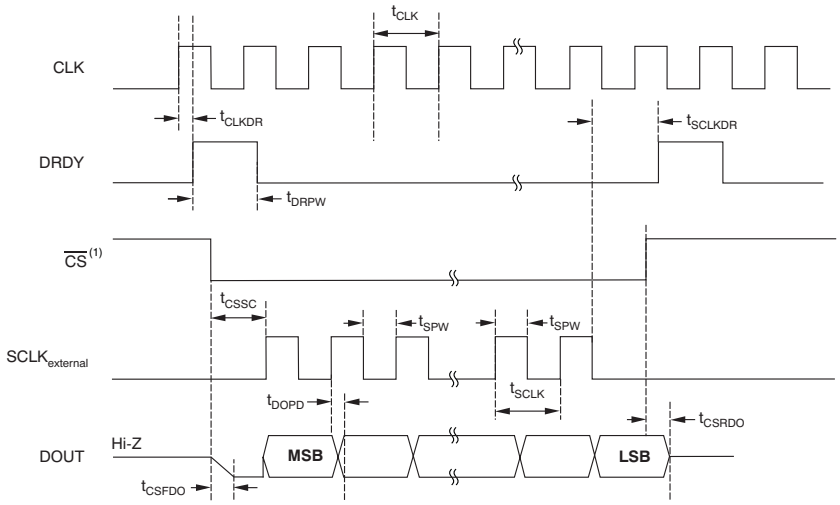


Figure 1. Data Retrieval Timing with Internal SCLK (SCLK_SEL = 0)

TIMING REQUIREMENTS: Internal SCLK

At T_A = –40°C to +85°C, and DVDD = 2.7V to 3.3V.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{CLK}	CLK period ($1/f_{CLK}$)	50			ns
t_{CLKDR}	CLK to DRDY delay		36		ns
t_{DRPW}	DRDY pulse width		1		t_{CLK}
t_{DRSCLK}	DRDY active edge to internally-generated SCLK rising edge		4		ns
t_{SCLK}	SCLK period ($1/f_{SCLK}$)		1		t_{CLK}
t_{DOPD}	Rising edge of SCLK to new valid data output (propagation delay)			3	ns
t_{DC}	CLK duty cycle	45		55	%
t_{SPWH}	SCLK pulse width high		20		ns



(1) $\overline{CS}$ may be tied low.

Figure 2. Data Retrieval Timing with External SCLK (SCLK_SEL = 1)

TIMING REQUIREMENTS: External SCLK

At T_A = –40°C to +85°C, and DVDD = 2.7V to 3.3V.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{CLK}	CLK period ($1/f_{CLK}$)	50			ns
t_{CLKDR}	CLK to DRDY delay		37		ns
t_{DRPW}	DRDY pulse width		1		t_{CLK}
t_{CSSC}	$\overline{CS}$ active low to first Shift Clock (setup time)	5			ns
t_{SCLK}	SCLK period ($1/f_{SCLK}$)	25			ns
t_{SPW}	SCLK high or low pulse width	12			ns
t_{DOPD}	Rising edge of SCLK to new valid data output (propagation delay)			11	ns
t_{SCLKDR}	Setup time of DRDY rising after SCLK falling edge	3			t_{CLK}
t_{CRSDO}	$\overline{CS}$ inactive to data output 3-state		8		ns

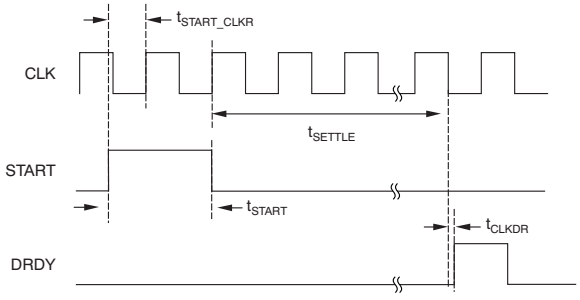


Figure 3. START Timing

TIMING REQUIREMENTS: START

At T_A = –40°C to +85°C, and DVDD = 2.7V to 3.3V.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{START_CLKR}	Setup time, rising edge of START to rising edge of CLK	0.5			t_{CLK}
t_{START}	Start pulse width	1			t_{CLK}

TYPICAL CHARACTERISTICS

All specifications are at T_A = –40°C to +85°C, AVDD = 5V, DVDD = 3V, f_{CLK} = 20MHz, V_{REF} = +3V, and R_{BIAS} = 7.5kΩ, unless otherwise noted.

OUTPUT SPECTRUM (1k, –0.5dBFS SIGNAL)

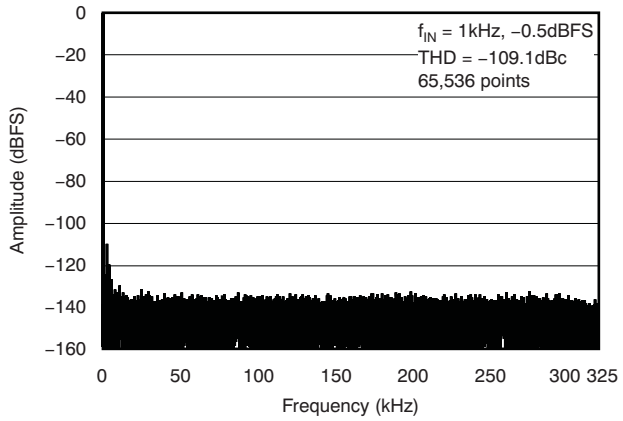


Figure 4.

OUTPUT SPECTRUM DETAIL VIEW (1k, –0.5dBFS SIGNAL)

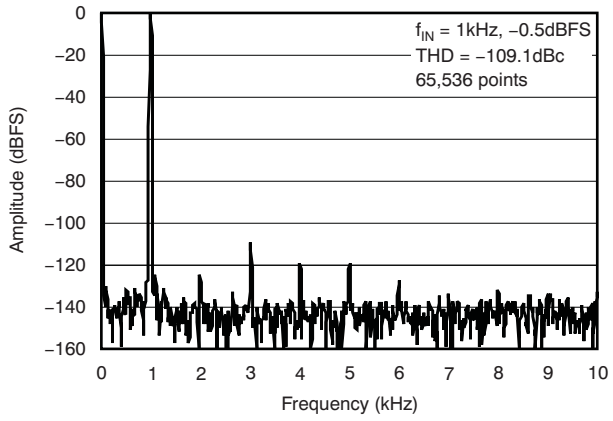


Figure 5.

OUTPUT SPECTRUM (1k, –6dBFS SIGNAL)

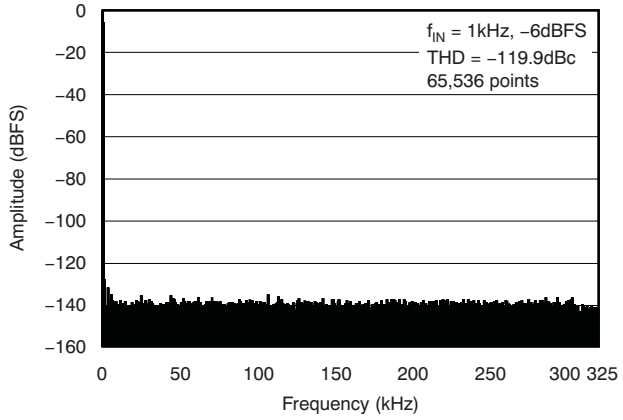


Figure 6.

OUTPUT SPECTRUM DETAIL VIEW (1k, –6dBFS SIGNAL)

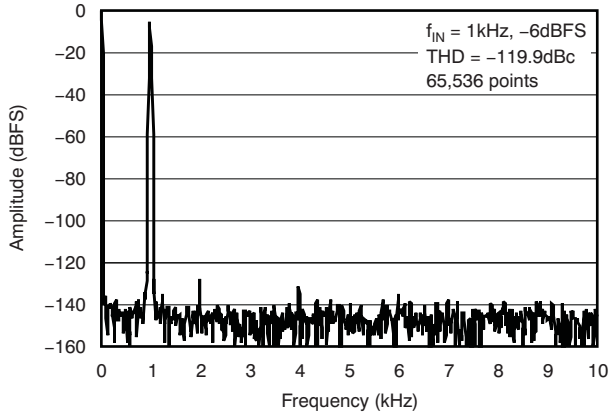


Figure 7.

OUTPUT SPECTRUM (10k, –0.5dBFS SIGNAL)

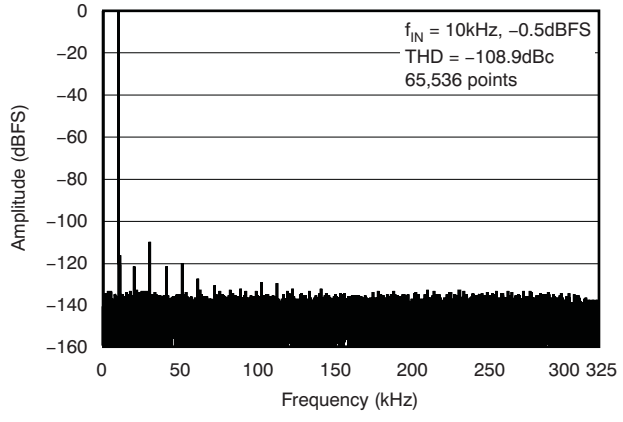


Figure 8.

OUTPUT SPECTRUM (10k, –6dBFS SIGNAL)

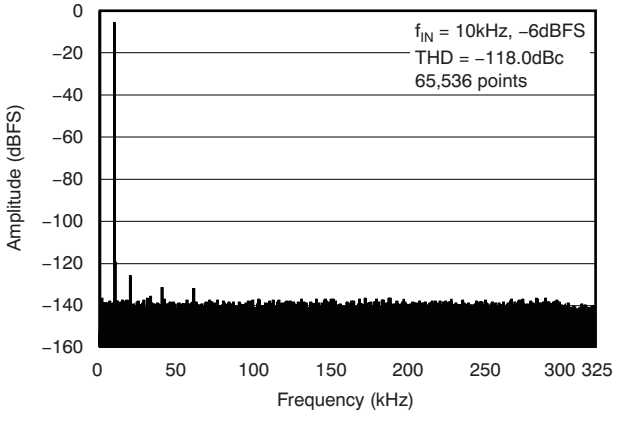


Figure 9.

TYPICAL CHARACTERISTICS (continued)

All specifications are at T_A = –40°C to +85°C, AVDD = 5V, DVDD = 3V, f_{CLK} = 20MHz, V_{REF} = +3V, and R_{BIAS} = 7.5kΩ, unless otherwise noted.

OUTPUT SPECTRUM (10k, –60dBFS SIGNAL)

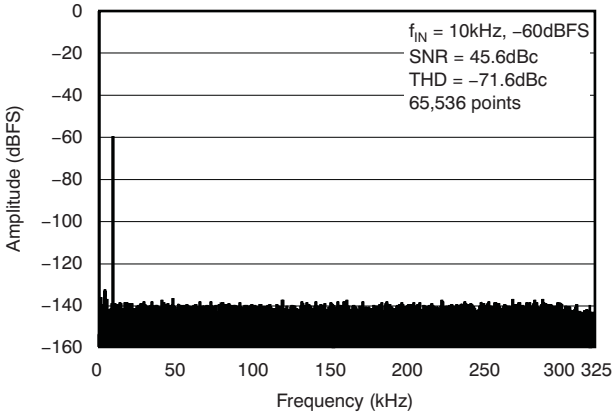


Figure 10.

SNR and |THD| vs INPUT FREQUENCY

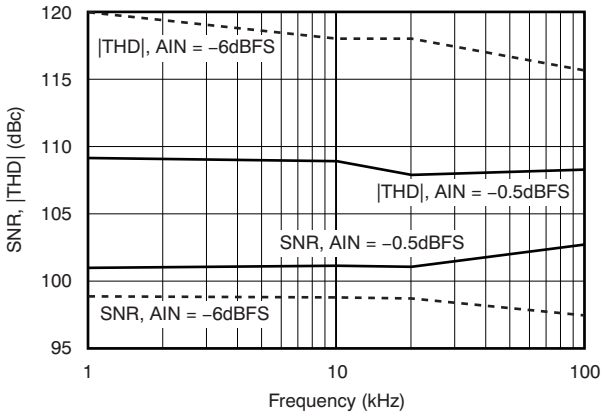


Figure 11.

SNR and |THD| vs SAMPLING FREQUENCY

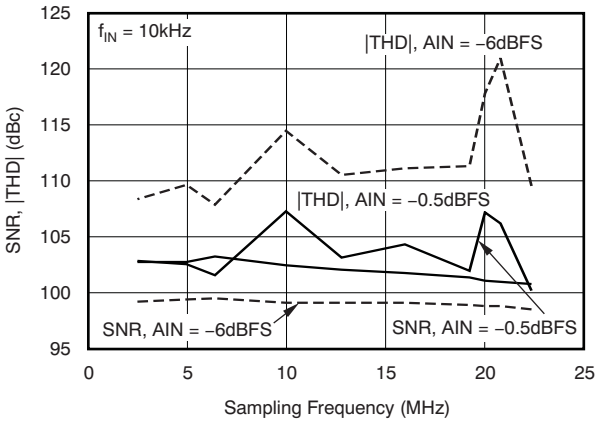


Figure 12.

SNR and |THD| vs INPUT AMPLITUDE

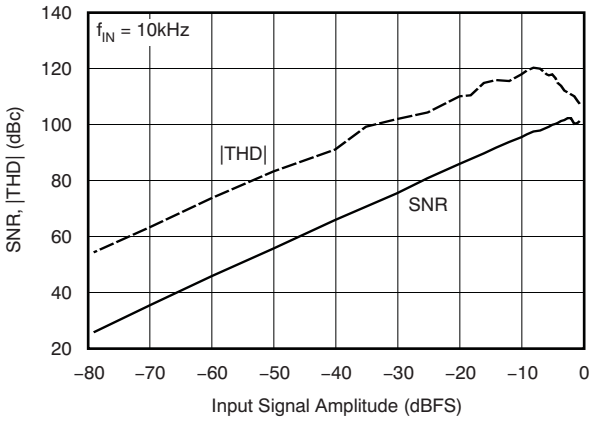


Figure 13.

SNR and |THD| vs INPUT COMMON-MODE

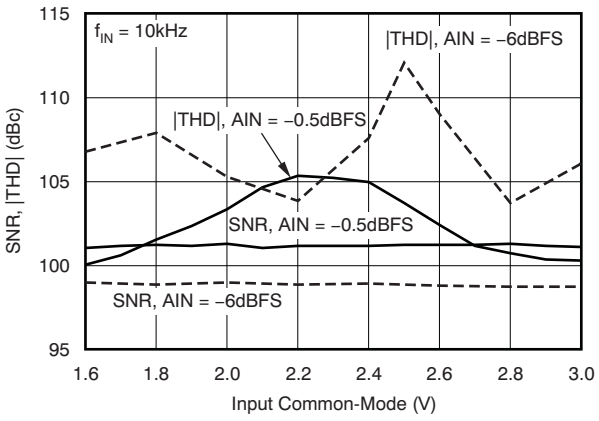


Figure 14.

SNR and |THD| vs TEMPERATURE

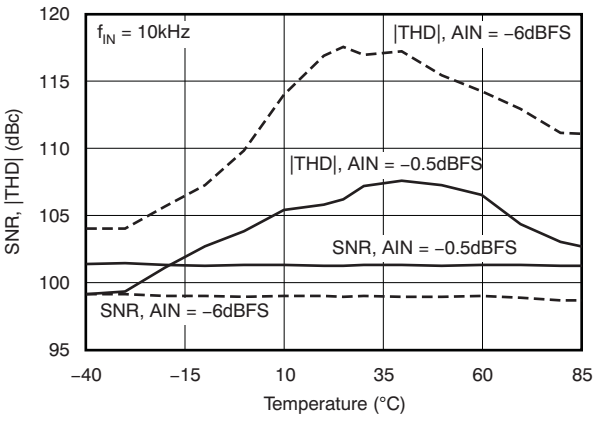


Figure 15.

TYPICAL CHARACTERISTICS (continued)

All specifications are at T_A = –40°C to +85°C, AVDD = 5V, DVDD = 3V, f_{CLK} = 20MHz, V_{REF} = +3V, and R_{BIAS} = 7.5kΩ, unless otherwise noted.

NOISE HISTOGRAM (OSR = 32)

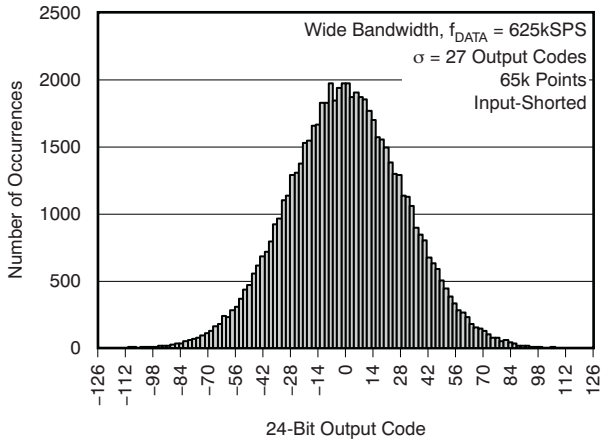


Figure 16.

NOISE HISTOGRAM (OSR = 256)

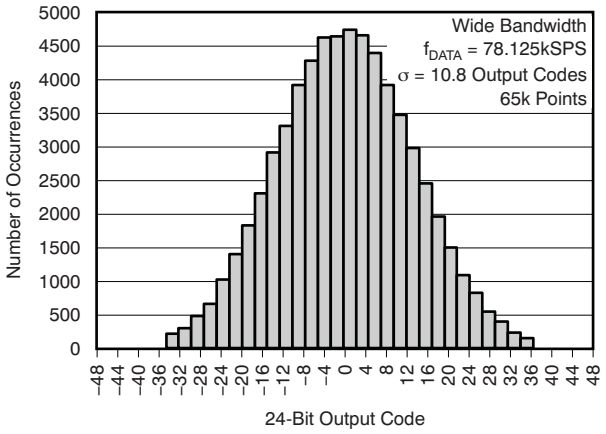


Figure 17.

DYNAMIC RANGE vs OVERSAMPLING RATIO

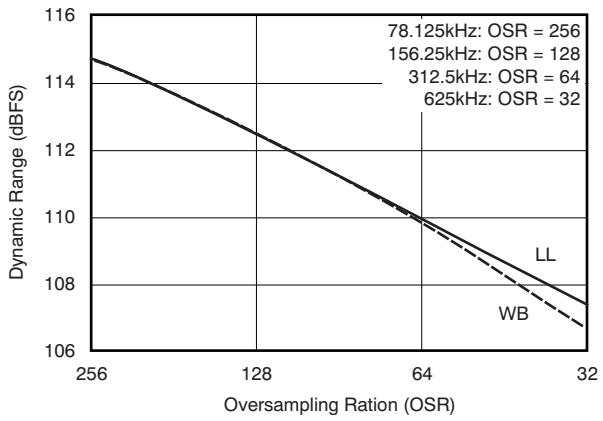


Figure 18.

NOISE vs INPUT VOLTAGE

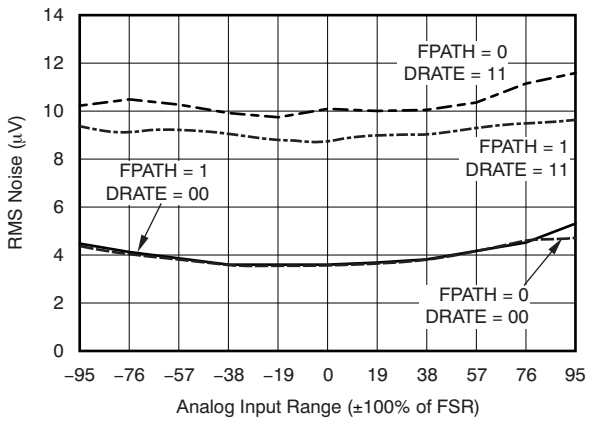


Figure 19.

INL vs TEMPERATURE

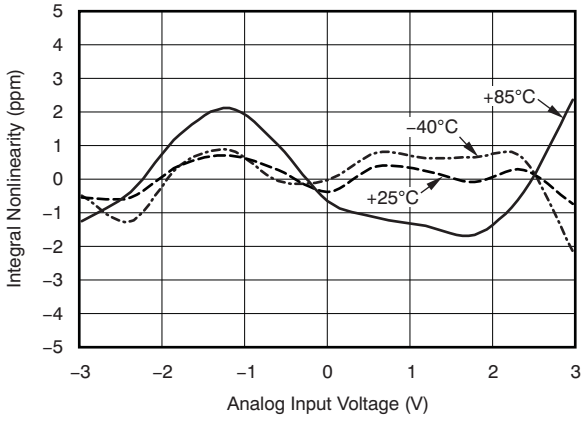


Figure 20.

|THD| vs R_{BIAS}

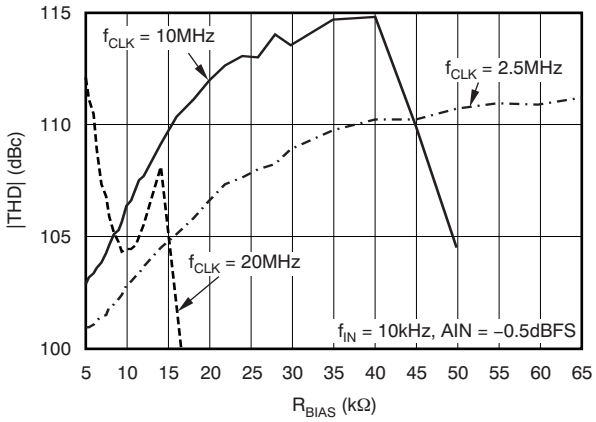


Figure 21.

TYPICAL CHARACTERISTICS (continued)

All specifications are at T_A = –40°C to +85°C, AVDD = 5V, DVDD = 3V, f_{CLK} = 20MHz, V_{REF} = +3V, and R_{BIAS} = 7.5kΩ, unless otherwise noted.

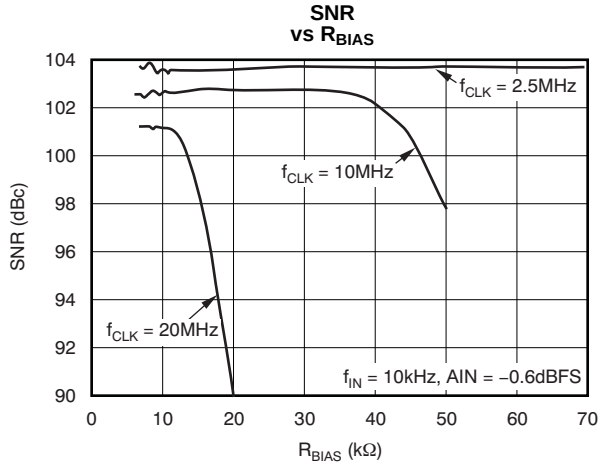


Figure 22.

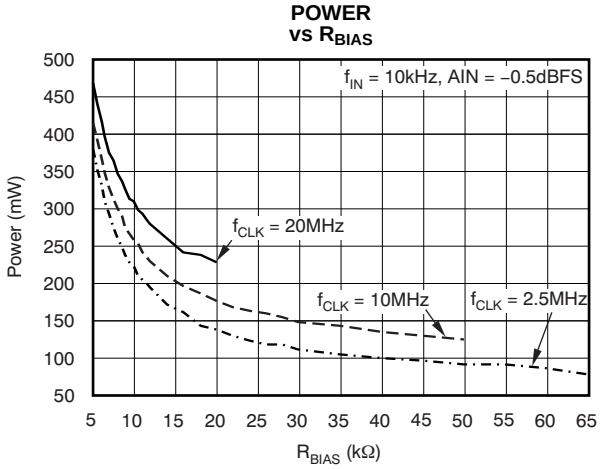


Figure 23.

OVERVIEW

The ADS1672 is a 24-bit, ΔΣ analog-to-digital converter (ADC). It provides high-resolution measurements of both ac and dc signals and features an advanced multi-stage analog modulator with a programmable and flexible digital decimation filter.

Figure 24 shows a block diagram of the ADS1672. The modulator is chopper-stabilized for low-drift performance and measures the differential input signal V_{IN} = (AINP – AINN) against the differential reference V_{REF} = (VREFP – VREFN). The digital filter receives the modulator signal and processes it through the user-selected path. The low-latency path provides single-cycle settling, and is ideal when using a multiplexer or when measuring large transients. The wide-bandwidth path provides outstanding frequency response with very low passband ripple, a steep transition band, and large stop band attenuation. This path is well-suited for applications that require high-resolution measurements of high-frequency ac signal content.

A dedicated START pin allows precise conversion control; toggle the pin to begin the conversion process. The ADS1672 is configured by setting the appropriate I/O pins—there are no registers to program. Data are retrieved over a serial interface that can support either CMOS or LVDS voltage levels. In addition, the serial interface can be internally or externally clocked. This flexibility allows direct connection to a wide range of digital hosts including DSPs, FPGAs, and microcontrollers.

A detection circuit monitors the conversions to indicate when the inputs are out-of-range for an extended duration. A power-down pin ($\overline{PDWN}$) shuts off all circuitry when the ADS1672 is not in use.

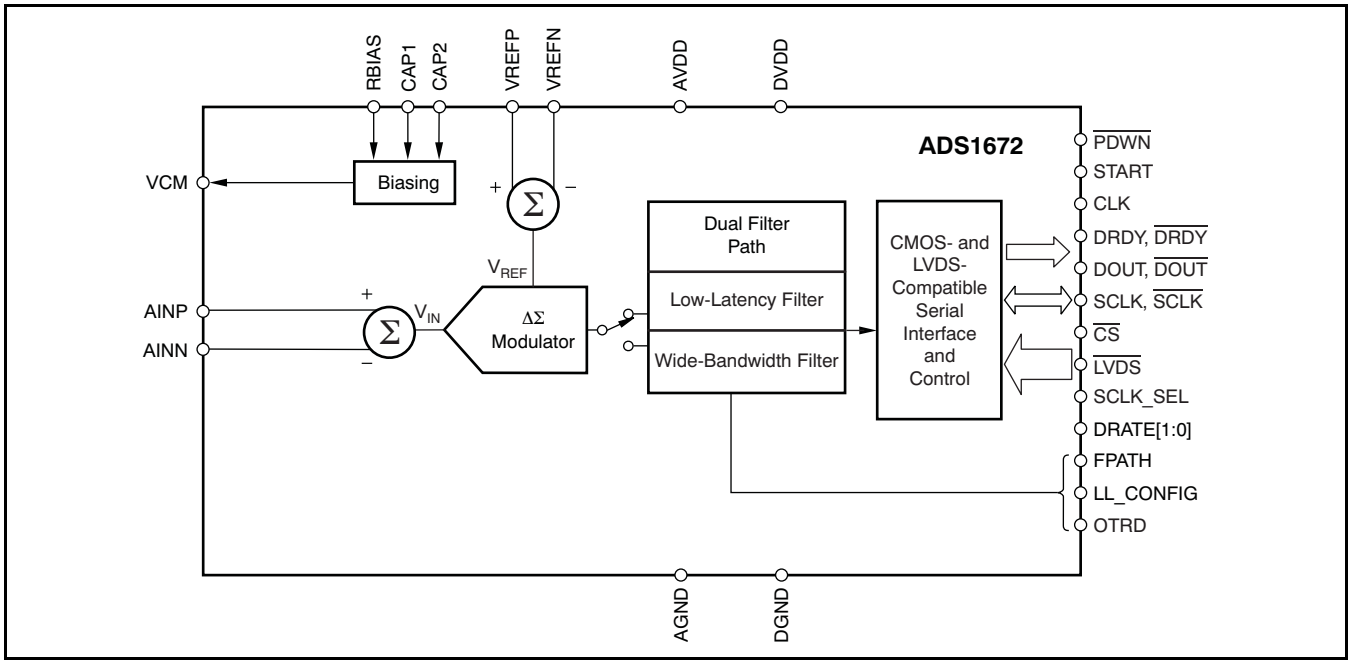


Figure 24. ADS1672 Block Diagram

NOISE PERFORMANCE

The ADS1672 offers outstanding noise performance that can be optimized by adjusting the data rate. As the averaging is increased (thus reducing the data rate), the noise drops correspondingly. Table 2 shows the noise as a function of data rate for both the low-latency and the wide-bandwidth filter paths under the conditions shown.

Table 2 lists some of the more common methods of specifying noise. The dynamic range is the ratio of the root-mean-square (RMS) value of a full-scale sine wave to the RMS noise with the inputs shorted together. This value is expressed in decibels relative to full-scale (dBFS). The input-referred noise is the RMS value of the noise with the inputs shorted, referred to the input of the ADS1672. The effective number of bits (ENOB) is calculated from a dc perspective using the formula in Equation 1, where full-scale range equals $2V_{REF}$.

$$ENOB = \frac{\ln\left(\frac{\text{Full-scale range}}{\text{RMS noise}}\right)}{\ln(2)} \quad (1)$$

Noise-free bits specifies noise, again from a dc perspective using Equation 1, with peak-to-peak noise substituted for RMS noise.

ANALOG INPUTS (AINP, AINN)

The ADS1672 measures the differential signal, V_{IN} = (AINP – AINN), against the differential reference, V_{REF} = (VREFP – VREFN). The most positive measurable differential input is V_{REF}, which produces the most positive digital output code of 7FFFFFh. Likewise, the most negative measurable differential input is $–V_{REF}$, which produces the most negative digital output code of 800000h.

Analog inputs must be driven with a differential signal to achieve optimum performance. The recommended common-mode voltage is 2.5V. The ADS1672 samples the analog inputs at very high speeds. It is critical that a suitable driver be used. See the *Application Information* section for recommended circuit designs.

Table 2. Noise Performance(1)

FILTER PATH	DATA RATE[1:0]	DATA RATE	DYNAMIC RANGE	INPUT-REFERRED NOISE	ENOB	NOISE-FREE BITS
Low-Latency (single-cycle settling configuration)	00	36kSPS	115dB	$3.9\mu V_{RMS}$	20.6	17.8
	01	68kSPS	113dB	$5.0\mu V_{RMS}$	20.2	17.5
	10	120kSPS	110dB	$6.7\mu V_{RMS}$	19.8	17.1
	11	180kSPS	108dB	$8.9\mu V_{RMS}$	19.4	16.7
Wide-Bandwidth	00	78.1kSPS	115.5dB	$3.9\mu V_{RMS}$	20.6	17.8
	01	156.3kSPS	113dB	$5.0\mu V_{RMS}$	20.2	17.5
	10	312.5kSPS	110dB	$6.8\mu V_{RMS}$	19.8	17.0
	11	625.0kSPS	107dB	$10.1\mu V_{RMS}$	19.2	16.5

(1) V_{REF} = 3V, f_{CLK} = 20MHz.

VOLTAGE REFERENCE INPUTS (VREFN, VREFP)

The voltage reference for the ADS1672 is the differential voltage between VREFP and VREFN:

V_{REF} = (VREFP – VREFN)

A high-quality reference voltage with the appropriate drive strength is essential for achieving the best performance from the ADS1672. Noise and drift on the reference degrade overall system performance. See the *Application Information* section for reference circuit examples.

It is recommended that a minimum 10µF and 0.1µF ceramic bypass capacitors be used directly across the reference inputs, VREFP and VREFN. These capacitors should be placed as close as possible to the device under test for optimal performance.

COMMON-MODE VOLTAGE (VCM)

The VCM pin outputs a voltage of AVDD/2 and can be used to set the common-mode output of the circuitry that drives the ADS1672. The pin must be bypassed with a 1µF capacitor placed close to the package pin, even if it is not connected elsewhere. The VCM pin has limited drive ability and therefore must be buffered if connected to a load.

CONVERSION START

The START pin provides an easy and precise conversion control. To perform a single conversion, pulse the START pin as shown in Figure 25. The START signal is latched internally on the rising edge of CLK. Multiple conversions are performed by continuing to hold START high after the first conversion completes; see the digital filter descriptions for more details on multiple conversions, because the timing depends on the filter path selected.

A conversion can be interrupted by issuing another START pulse before the ongoing conversion completes. When an interruption occurs, the data for the ongoing conversion are flushed and a new conversion begins. DRDY indicates that data are ready for retrieval after the filter has settled, as shown in Figure 26.

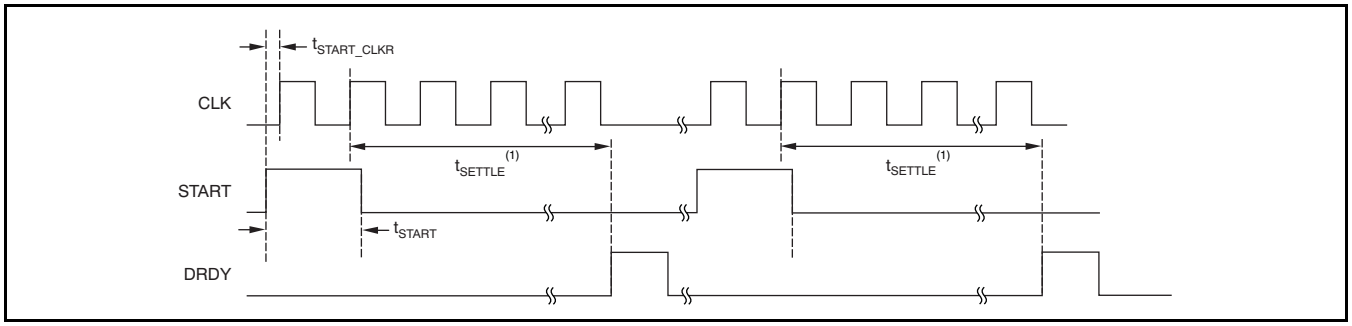
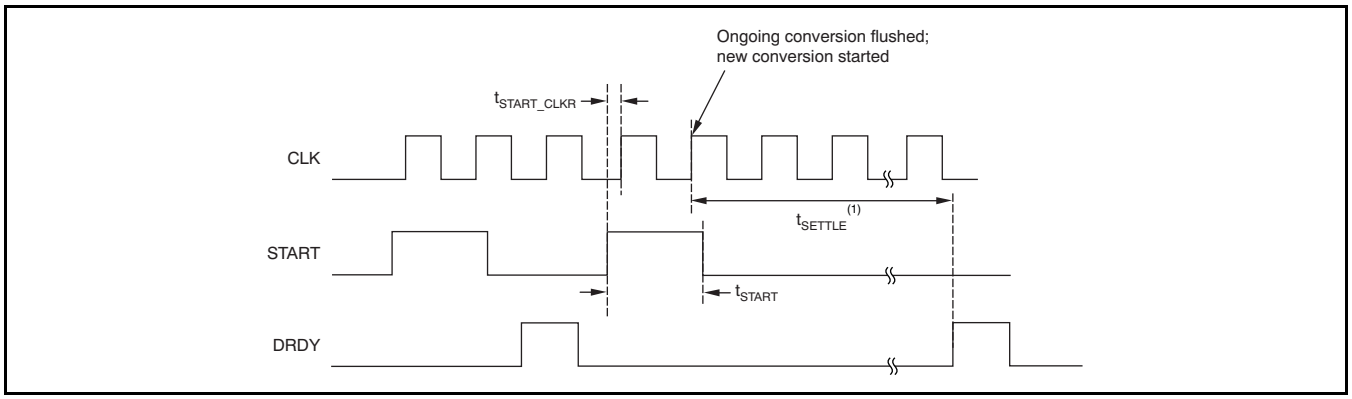


Figure 25. START Pin Used for Single Conversions



(1) See Low-Latency Filter section and Wide Bandwidth Filter section for specific values of settling time t_{SETTLE}.

Figure 26. Example of Restarting a Conversion with START

DIGITAL FILTER

In delta-sigma ADCs, the digital filter has a critical influence on device performance. The digital filter sets the frequency response, data rate, bandwidth, and settling time. Choosing to optimize some of these features in a filter means that compromises must be made with other specifications. These tradeoffs determine the applications for which the device is best suited.

The ADS1672 offers two digital filters on-chip, and allows the user to direct the output data from the modulator to either the Wide-Bandwidth or Low-Latency filter. These filters allow the user to use one converter design to address multiple applications. The Low-Latency path filter has minimal latency or settling time. This path is ideal for measurements with large, quick changes on the inputs (for example, when using a multiplexer). The low-latency characteristic allows the user to cycle through the multiplexer at high speeds. The frequency characteristics are relaxed in order to provide the low latency.

The other path provides a filter with excellent frequency response characteristics. The passband ripple is extremely small, the transition band is very steep, and there is large stop band attenuation. These characteristics are needed for high-resolution measurements of ac signals. The tradeoff here is that settling time increases; but for signal processing, this increase is not generally a critical concern.

The FPATH digital input pin sets the filter path selection, as shown in Table 3. Note that the START pin must be strobed after a change to the filter path selection or data rate. If a conversion is in process during a filter path or data rate change, the output data are not valid and should be discarded.

Table 3. ADS1672 Filter Path Selection

FPATH PIN	SELECTED FILTER PATH
1	Low-latency path
0	Wide-bandwidth path

LOW-LATENCY DIGITAL FILTER

The low-latency (LL) filter provides a fast settling response targeted for applications that need high-precision measurements with minimal latency. A good example of this type of application is using a multiplexer to measure multiple inputs. The faster that the ADC settles, the faster the measurement can complete and the multiplexer can advance to the next input.

The ADS1672 LL filter supports two configurations to help optimize performance for these types of applications.

The LL_CONFIG input pin selects the configuration, as shown in Table 4. Be sure to strobe the START pin after changing the configuration. If a conversion is in process during a configuration change, the output data for that conversion are not valid and should be discarded.

Table 4. Low-Latency Pin Configurations

LL_CONFIG PIN	LOW-LATENCY CONFIGURATION
0	Single-cycle settling
1	Fast response

The first configuration is *single-cycle settling*. As the name implies, this configuration allows for the filter to completely settle in one conversion cycle; there is no need to discard data. Each data output is comprised of information taken during only the previous conversion. The DRATE[1:0] digital input pins select the data rate for the Single-Cycle Settling configuration, as shown in Table 5. Note that the START pin must be strobed after a change to the data rate. If a conversion is in process during a data rate change, the output data for that conversion are not valid and should be discarded.

Table 5. Low-Latency Data Rates with Single-Cycle Settling Configuration

DRATE[1:0]	DATA RATE ($1/t_{DRDY-SCS}$)	SETTLING TIME, $t_{SETTLE-LL}$		–3dB BANDWIDTH(1)
00	36.30kSPS	27.55µs	550 t_{CLK}	34kHz
01	67.80kSPS	14.75µs	294 t_{CLK}	68kHZ
10	119.76kSPS	8.35µs	166 t_{CLK}	130kHZ
11	180.18kSPS	5.55µs	110 t_{CLK}	215kHz

(1) The input signal aliases when its frequency exceeds $f_{DATA}/2$, in accordance with the Nyquist theorem.

The second configuration is *fast response*. The DRATE[1:0] digital input pins select the data rate for the Fast Response Configuration, as shown in Table 6. When selected, this configuration provides a higher output data rate. The faster output data rate allows for more averaging by a post-processor within a given time interval to reduce noise. It also provides a faster indication of changes on the inputs when monitoring quickly-changing signals (for example, in a control loop application).

Table 6. Low-Latency Data Rates with Fast-Response Configuration

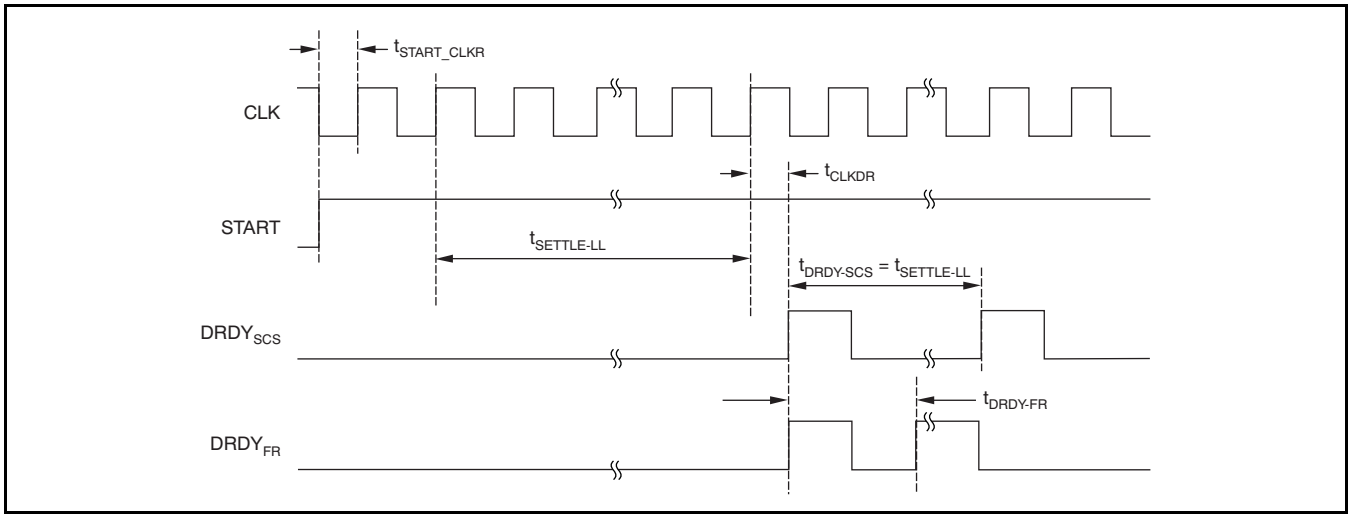
DRATE [1:0]	DATA RATE ($1/t_{DRDY-FR}$)	SETTLING TIME, $t_{SETTLE-LL}$		–3dB BANDWIDTH
00	78.125kSPS	27.55µs	550 t_{CLK}	34kHz
01	156.25kSPS	14.75µs	294 t_{CLK}	68kHZ
10	312.5kSPS	8.35µs	166 t_{CLK}	130kHZ
11	625kSPS	5.55µs	110 t_{CLK}	215kHz

Settling Time

The settling time in absolute time (µs) is the same for both configurations of the low-latency filter, as shown in Table 5 and Table 6. The difference between the configurations is seen with the timing of the conversions after the filter has settled from a pulse on the START pin.

Figure 27 illustrates the response of both configurations on approximately the same time scale in order to highlight the differences. With the single-cycle settling configuration, each conversion fully settles; in other words, the conversion period $t_{DRDY-SCS} = t_{SETTLE-LL}$. The benefit of this configuration is its simplicity—the ADS1672 functions similar to a SAR converter and there is no need to consider discarding partially-settled data because each conversion is fully settled.

With the fast response configuration, the data rate for conversions after initial settling is faster; that is, the conversion time is less than the settling: $t_{DRDY-FR} < t_{SETTLE-LL}$. One benefit of this configuration is a faster response to changes on the inputs, because data are supplied at a faster rate. Another advantage is better support for post-processing. For example, if multiple readings are averaged to reduce noise, the higher data rate of the fast response configuration allows this averaging to happen in less time than it requires with the single-cycle settling filter. A third benefit is the ability to measure higher input frequencies without aliasing as a result of the higher data rate.



NOTE: $DRDY_{SCS}$ is the DRDY output with the low-latency single-cycle settling configuration. $DRDY_{FR}$ is the DRDY output with the low-latency fast-response settling configuration.

Figure 27. Low-Latency Single-Cycle Settling and Fast-Response Configuration Conversion Timing

It is important to note, however, that the absolute settling time of the low-latency path does not change when using the fast response configuration. Changes on the input signal during conversions after the initial settling require multiple cycles to fully settle. To help illustrate this requirement, consider a change on the inputs as shown in Figure 31, where START is assumed to have been taken high before the input voltage was changed.

The readings after the input change settle as shown in Figure 28. Conversion 3 provides a fully-settled result at the new V_{IN} signal.

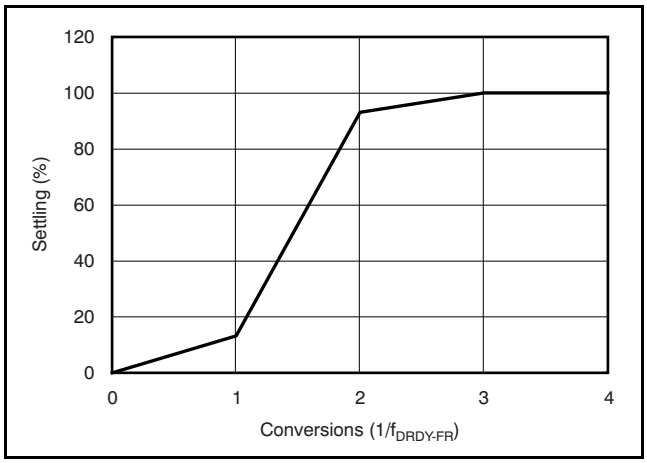


Figure 28. Step Response for Low-Latency Filter with Fast-Response Configuration

Frequency Response

Figure 29 shows the frequency response for the low-latency filter path normalized to the output data rate, f_{DATA}. The overall frequency response repeats at the modulator sampling rate, which is the same as the input clock frequency. Figure 30 shows the response with the fastest data rate selected (625kSPS when f_{CLK} = 20MHz).

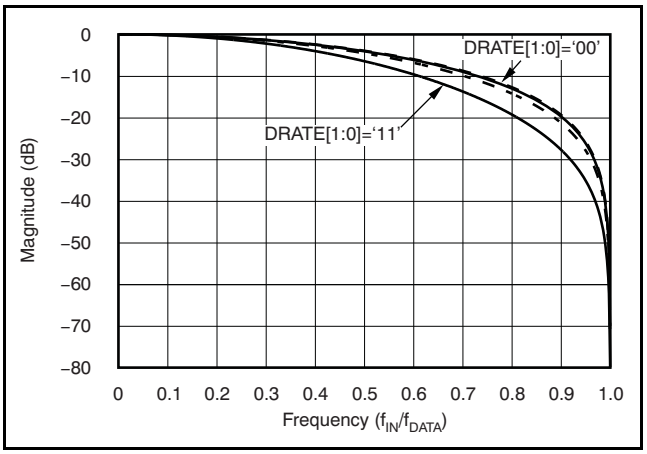


Figure 29. Frequency Response of Low-Latency Filter in Fast-Response Configuration

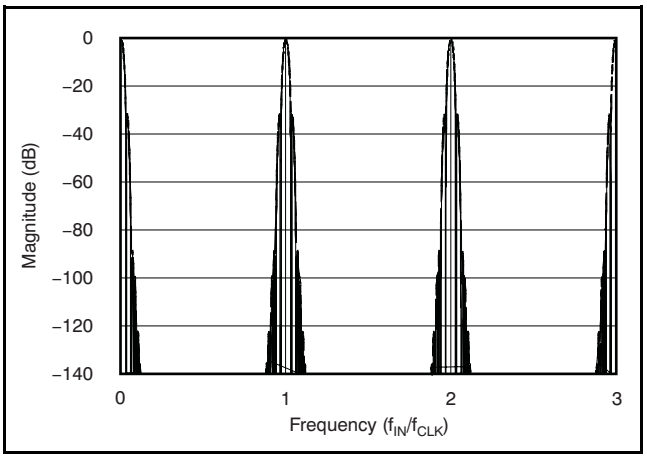
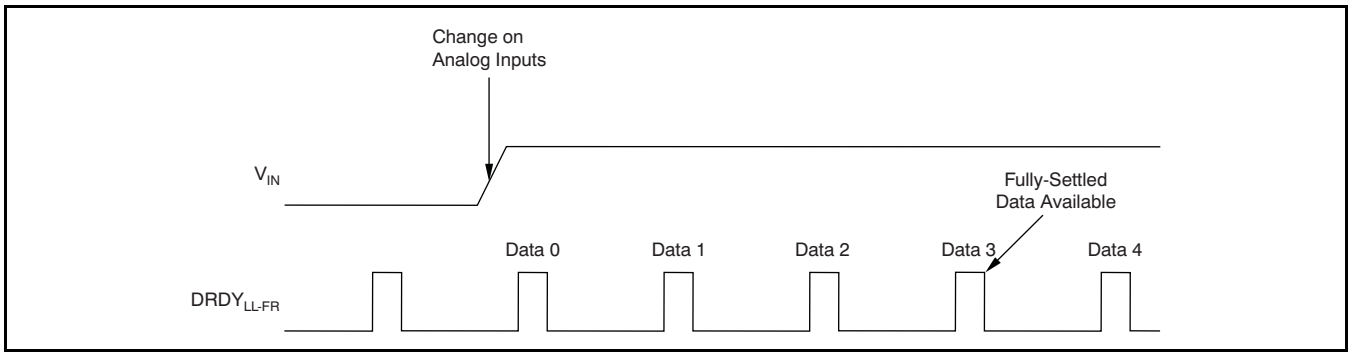


Figure 30. Extended Frequency Response of Low-Latency Path



NOTE: START pin held high previous to change on analog inputs.

Figure 31. Settling Example with the Low-Latency Filter in Fast-Response Configuration

Phase Response

The low-latency filter uses a multiple stage linear phase digital filter. Linear phase filters exhibit constant delay time versus input frequency (also know as *constant group delay*). This feature of linear phase filters means that the time delay from any instant of the input signal to the corresponding same instant of the output data is constant and independent of the input signal frequency. This behavior results in essentially zero phase error when measuring multi-tone signals.

WIDE-BANDWIDTH FILTER

The wide-bandwidth (WB) filter is well-suited for measuring high-frequency ac signals. This digital filter offers excellent passband and stop band characteristics.

The DRATE[1:0] digital input pins select from the four data rates available with the WB filter, as shown in Table 7. Note that the START pin must be strobed after a change to the data rate. If a conversion is in process during a data rate change, the output data for that conversion are not valid and should be discarded.

Table 7. Wide-Bandwidth Data Rates

DRATE [1:0]	DATA RATE ($1/t_{DRDY-WB}$)	–3dB BANDWIDTH	SETTLING TIME, $t_{SETTLE-WB}$	
00	78.125kSPS	38kHz	704µs	14061 t_{CLK}
01	156.25kSPS	76kHz	352µs	7033 t_{CLK}
10	312.50kSPS	152kHz	176µs	3519 t_{CLK}
11	625.0kSPS	305kHz	88µs	1762 t_{CLK}

While using the wide-bandwidth filter path, the LL_CONFIG pin must be set to logic HIGH. Setting LL_CONFIG to a logic low forces the ADS1672 to switch to the low-latency filter path, single cycle settling mode overriding FPATH pin.

Frequency Response

Figure 32 shows the frequency response for the wide-bandwidth filter path normalized to the output data rate, f_{DATA}. Figure 33 shows the passband ripple, and the transition from passband to stop band is illustrated in Figure 34. These three plots are valid for all of the data rates available on the ADS1672. Simply substitute the selected data rate to express the x-axis in absolute frequency.

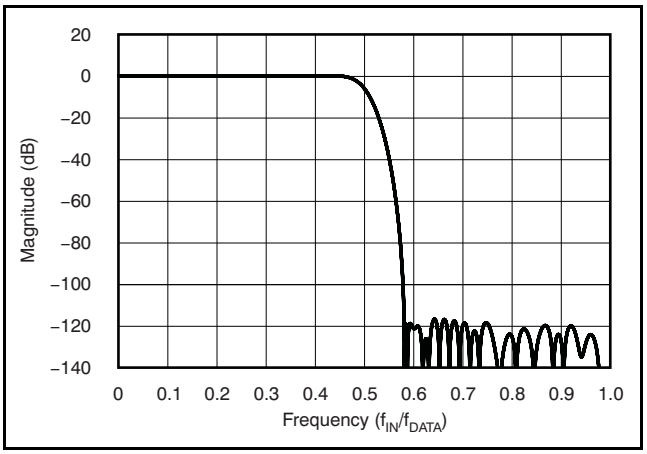


Figure 32. Frequency Response of Wide-Bandwidth Filter

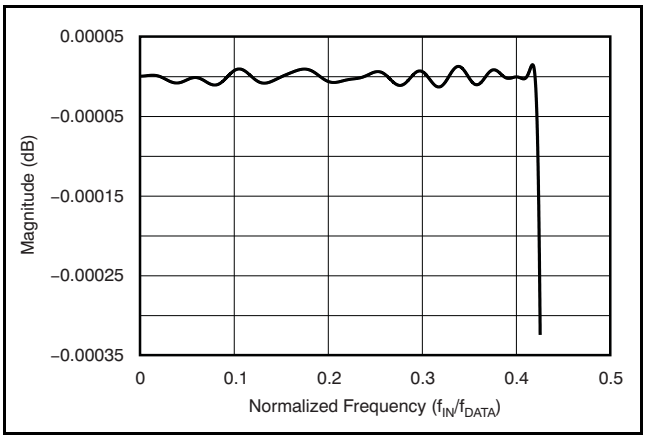


Figure 33. Passband Response for Wide-Bandwidth Filter

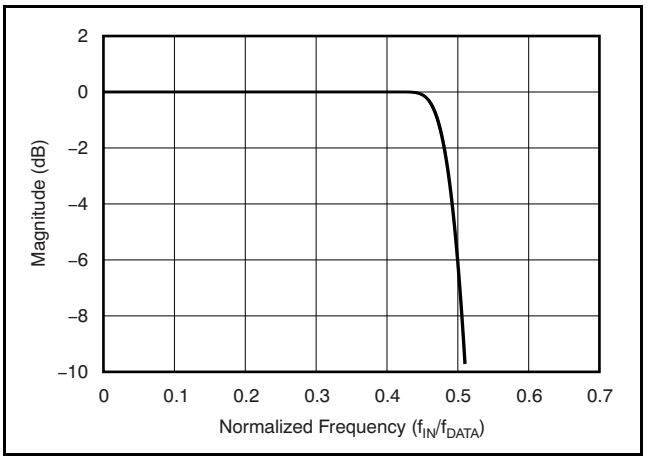


Figure 34. Transition Band Response for Wide-Bandwidth Filter

The overall frequency response repeats at the modulator sampling rate, which is the same as the input clock frequency. Figure 35 shows the response with the fastest data rate selected (625kSPS when f_{CLK} = 20MHz).

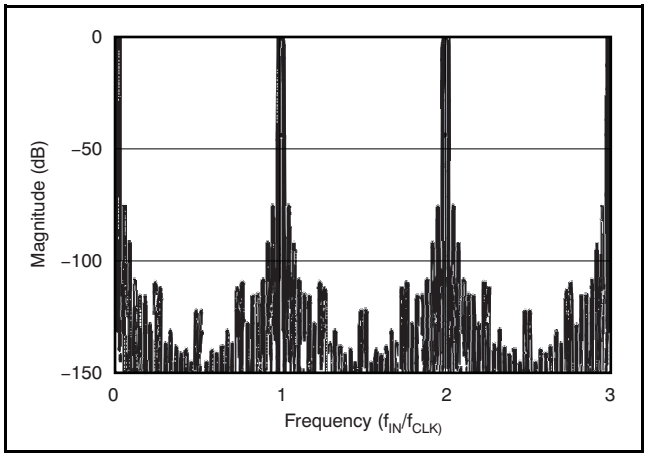


Figure 35. Extended Frequency Response of Wide-Bandwidth Path

Phase Response

The wide-bandwidth filter uses a multiple-stage, linear-phase digital filter. Linear phase filters exhibit constant delay time versus input frequency (also know as *constant group delay*). This feature means that the time delay from any instant of the input signal to the corresponding same instant of the output data is constant and independent of the input signal frequency. This behavior results in essentially zero phase error when measuring multi-tone signals.

Settling Time

The Wide-Bandwidth filter fully settles before indicating data are ready for retrieval after the START pin is taken high, as shown in Figure 37. For this filter, the settling time is larger than the conversion time: $t_{SETTLE-WB}$ > $t_{DRDY-WB}$. Instantaneous steps on the input require multiple conversions to settle if START is not pulsed. Figure 36 shows the settling response with the x-axis normalized to conversions or data-ready cycles. The output is fully settled after 55 data-ready cycles.

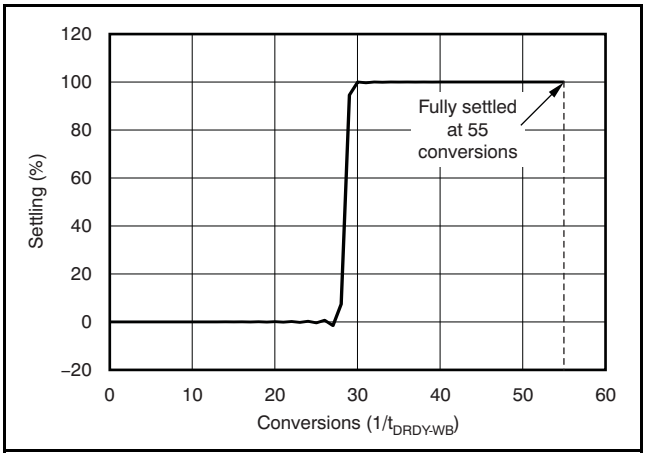
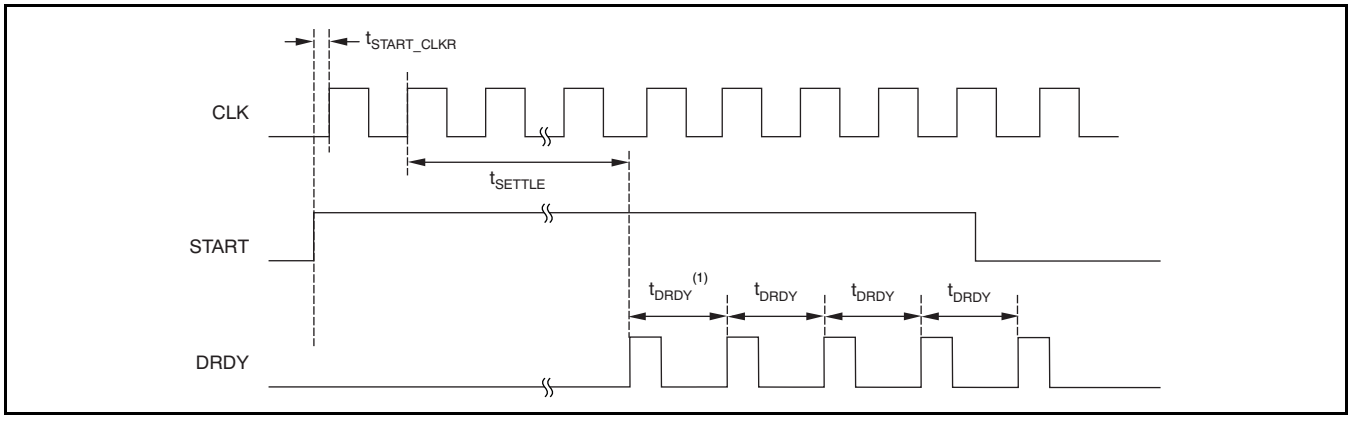


Figure 36. Step Response for Wide-Bandwidth Filter



(1) t_{DRDY} = $1/f_{DATA}$. See Table 7 for the relationship between t_{SETTLE} and t_{DRDY} when using the Wide-Bandwidth filter.

Figure 37. START Pin Used for Multiple Conversions with Wide-Bandwidth Filter Path

OTRD FUNCTION

The ADS1672 provides an out-of-range (OTRD) pin that can be used in feedback loops to set the dynamic range of the input signal.

The OTRD function is triggered when the output code of the digital filter exceeds the positive or negative full-scale range. OTRD goes high on the rising edge of DRDY. When the digital output code returns within the full-scale range, OTRD returns low on the next rising edge of DRDY. OTRD can also be used when small out-of-range input glitches must be ignored.

SERIAL INTERFACE

The ADS1672 offers a flexible and easy-to-use, read-only serial interface designed to connect to a wide range of digital processors, including DSPs, microcontrollers, and FPGAs. The ADS1672 serial interface can be configured to support either standard CMOS voltage swings or low-voltage differential swings (LVDS). In addition, when using standard CMOS voltage swings, SCLK can be internally or externally generated.

The ADS1672 is entirely controlled by pins; there are no registers to program. Connect the I/O pins to the appropriate level to set the desired function. Whenever changing the I/O pins that are used to control the ADS1672, be sure to issue a START pulse immediately after the change in order to latch the new values.

USING LVDS OUTPUT SWINGS

When the $\overline{\text{LVDS}}$ pin is set to '0', the ADS1672 outputs are LVDS TIA/EIA-644A compliant. The data out, shift clock, and data ready signals are output on the differential pairs of pins DOUT/$\overline{\text{DOUT}}$, SCLK/$\overline{\text{SCLK}}$, and DRDY/$\overline{\text{DRDY}}$, respectively. The voltage on the outputs is centered on 1.2V and swings approximately 350mV differentially. For more information on the LVDS interface, refer to the document Low-Voltage Differential Signaling (LVDS) Design Notes (literature number SLLA014) available for download at www.ti.com.

When using LVDS, the $\overline{\text{CS}}$ function is not available and SCLK must be internally generated. The states of the $\overline{\text{CS}}$ and SCLK_SEL pins are ignored, but do not leave these pins floating; they must be tied high or low.

USING CMOS OUTPUT SWINGS

When the $\overline{\text{LVDS}}$ pin is set to '1', the ADS1672 outputs are CMOS-compliant and swing from rail to rail. The data out and data ready signals are output on the differential pairs of pins DOUT/$\overline{\text{DOUT}}$ and DRDY/$\overline{\text{DRDY}}$, respectively. Note that these are the same pins used to output LVDS signals when the $\overline{\text{LVDS}}$ pin is set to '0'. $\overline{\text{DOUT}}$ and $\overline{\text{DRDY}}$ are complementary outputs provided for convenience. When not in use, these pins should be left floating.

See the *Serial Shift Clock* section for a description of the SCLK and $\overline{\text{SCLK}}$ pins.

DATA OUTPUT (DOUT, $\overline{\text{DOUT}}$)

Data are output serially from the ADS1672, MSB first, on the DOUT and $\overline{\text{DOUT}}$ pins. When LVDS signal swings are used, these two pins act as a differential pair to produce the LVDS-compatible differential output signal. When CMOS signal swings are used, the $\overline{\text{DOUT}}$ pin is the complement of DOUT. If $\overline{\text{DOUT}}$ is not used, it should be left floating.

DATA READY (DRDY, $\overline{\text{DRDY}}$)

Data ready for retrieval are indicated on the DRDY and $\overline{\text{DRDY}}$ pins. When LVDS signal swings are used, these two pins act as a differential pair to produce the LVDS-compatible differential output signal. When CMOS signal swings are used, the $\overline{\text{DRDY}}$ pin is the complement of DRDY. If one of the data ready pins is not used when CMOS swings are selected, it should be left floating.

SERIAL SHIFT CLOCK (SCLK, $\overline{SCLK}$, SCLK_SEL)

The serial shift clock SCLK is used to shift out the conversion data, MSB first, onto the Data Output pins. Either an internally- or externally-generated shift clock can be selected using the SCLK_SEL pin. If SCLK_SEL is set to '0', a free-running shift clock is generated internally from the master clock and outputs on the SCLK and $\overline{SCLK}$ pins. The $\overline{LVDS}$ pin determines if the output voltages are CMOS or LVDS. If SCLK_SEL is set to '1' and $\overline{LVDS}$ is set to '1', the SCLK pin is configured as an input to accept an externally-generated shift clock. In this case, the $\overline{SCLK}$ pin always outputs low. When SCLK_SEL is set to '0', the SCLK and $\overline{SCLK}$ pins are configured as outputs, and the shift clock is generated internally using the master clock input (CLK).

When LVDS signal swings are used, the shift clock is automatically generated internally regardless of the state of SCLK_SEL. In this case, SCLK_SEL cannot be left floating; it must be tied high or low.

Table 8 summarizes the ADS1672 supported serial clock configurations.

Table 8. Supported Serial Clock Configurations

DIGITAL OUTPUTS	SHIFT CLOCK (SCLK)
LVDS	Must be generated internally
CMOS	Internal (SCLK_SEL = '0')
	External (SCLK_SEL = '1')

CHIP SELECT ($\overline{CS}$)

The chip select input ($\overline{CS}$) allows multiple devices to share a serial bus. When $\overline{CS}$ is inactive (high), the serial interface is reset and the data output pins DOUT and $\overline{DOUT}$ enter a high-impedance state. SCLK is internally generated; the SCLK and $\overline{SCLK}$ output pins also enter a high-impedance state when $\overline{CS}$ is inactive. The DRDY and $\overline{DRDY}$ outputs are always active, regardless of the state of the $\overline{CS}$ output. $\overline{CS}$ may be permanently tied low when the outputs do not share a bus.

DATA FORMAT

The ADS1672 outputs 24 bits of data in two's complement format. A positive full-scale input produces an output code of 7FFFFFh, and the negative full-scale input produces an output code of 800000h. The output clips at these codes for signals exceeding full-scale. Table 9 summarizes the ideal output codes for different input signals. When the input is positive out-of-range, exceeding the positive full-scale value of V_{REF}, the output clips to all 7FFFFFh. Likewise, when the input is negative out-of-range by going below the negative full-scale value of $-V_{REF}$, the output clips to 800000h.

Table 9. Ideal Output Code vs Input Signal

INPUT SIGNAL V_{IN} = (AINP – AINN)	IDEAL OUTPUT CODE(1)
$\geq V_{REF}$	7FFFFFh
$\frac{+V_{REF}}{2^{23} - 1}$	000001h
0	000000h
$\frac{-V_{REF}}{2^{23} - 1}$	FFFFFFh
$\leq -V_{REF}\left(\frac{2^{23}}{2^{23} - 1}\right)$	8000000h

1. Excludes effects of noise, INL, offset and gain errors.

CLOCK INPUT (CLK)

The ADS1672 requires that an external clock signal be applied to the CLK input pin. The sampling of the modulator is controlled by this clock signal. As with any high-speed data converter, a high-quality clock is essential for optimum performance. Crystal clock oscillators are the recommended CLK source; other sources, such as frequency synthesizers, are usually inadequate. Make sure to avoid excess ringing on the CLK input; keep the trace as short as possible.

Measuring high-frequency, large amplitude signals requires tight control of clock jitter. The uncertainty during sampling of the input from clock jitter limits the maximum achievable SNR. This effect becomes more pronounced with higher frequency and larger magnitude inputs. Fortunately, the ADS1672 oversampling topology reduces clock jitter sensitivity over that of Nyquist rate converters, such as pipeline and successive approximation converters, by at least a factor of $\sqrt{32}$.

For best performance, the duty cycle of CLK should be very close to 50%. The rise and fall times of the clock should be less than 2ns and the clock amplitude should be equal to AVDD.

SYNCHRONIZING MULTIPLE ADS1672s

The START pin should be applied at power-up and resets the ADS1672 filters. START begins the conversion process, and the START pin enables simultaneous sampling with multiple ADS1672s in multichannel systems. All devices to be synchronized must use a common CLK input.

It is recommended that the START pin be aligned to the falling edge of CLK to ensure proper synchronization because the START signal is internally latched by the ADS1672 on the rising edge of CLK.

With the CLK inputs running, pulse START on the falling edge of CLK, as shown in Figure 38. Afterwards, the converters operate synchronously with the $\overline{\text{DRDY}}$ outputs updating simultaneously. After synchronization, $\overline{\text{DRDY}}$ is held high until the digital filter has fully settled.

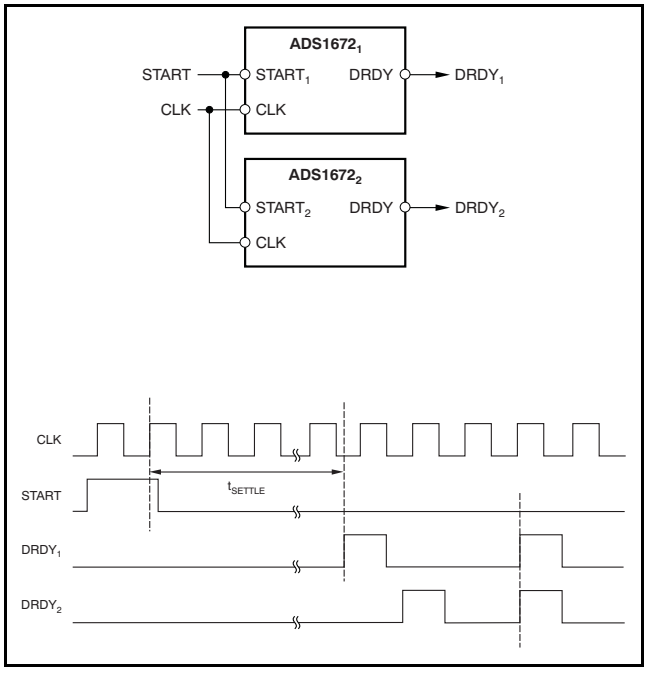


Figure 38. Synchronizing Multiple Converters

ANALOG POWER DISSIPATION

An external resistor connected between the RBIAS pin and the analog ground sets the analog current level, as shown in Figure 39. The current is inversely proportional to the resistor value. Figure 21 and Figure 23 (in the Typical Characteristics) show power and typical performance at values of R_{BIAS} for different CLK frequencies. Notice that the analog current can be reduced when using a slower frequency CLK input because the modulator has more time to settle. Avoid adding any capacitance in parallel to R_{BIAS}, because this additional capacitance interferes with the internal circuitry used to set the biasing.

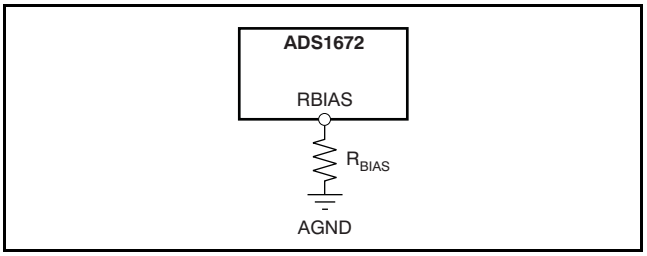


Figure 39. External Resistor Used to Set Analog Power Dissipation (Depends on f_{CLK})

POWER DOWN ($\overline{\text{PDWN}}$)

When not in use, the ADS1672 can be powered down by taking the $\overline{\text{PDWN}}$ pin low. All circuitry shuts down, including the voltage reference. To minimize the digital current during power down, stop the clock signal supplied to the CLK input. Make sure to allow time for the reference to start up after exiting power-down mode.

After the reference has stabilized, allow for the modulator and digital filter to settle before retrieving data.

POWER SUPPLIES

Two supplies are used on the ADS1672: analog (AVDD) and digital (DVDD). Each supply must be suitably bypassed to achieve the best performance. It is recommended that a 1µF and 0.1µF ceramic capacitor be placed as close to each supply pin as possible. Connect each supply-pin bypass capacitor to the associated ground. Each main supply bus should also be bypassed with a bank of capacitors from 47µF to 0.1µF. Figure 40 illustrates the recommended method for ADS1672 power-supply decoupling.

Power-supply pins 53 and 54 are used to drive internal clock supply circuits and, as a result, are generally very noisy. It is highly recommended that traces from these pins not be shared or run close to any of the adjacent AVDD or AGND pins of the ADS1672. These pins should be well-decoupled, using a 0.1µF ceramic capacitor placed close to the pins, and immediately terminated into the power and ground planes.

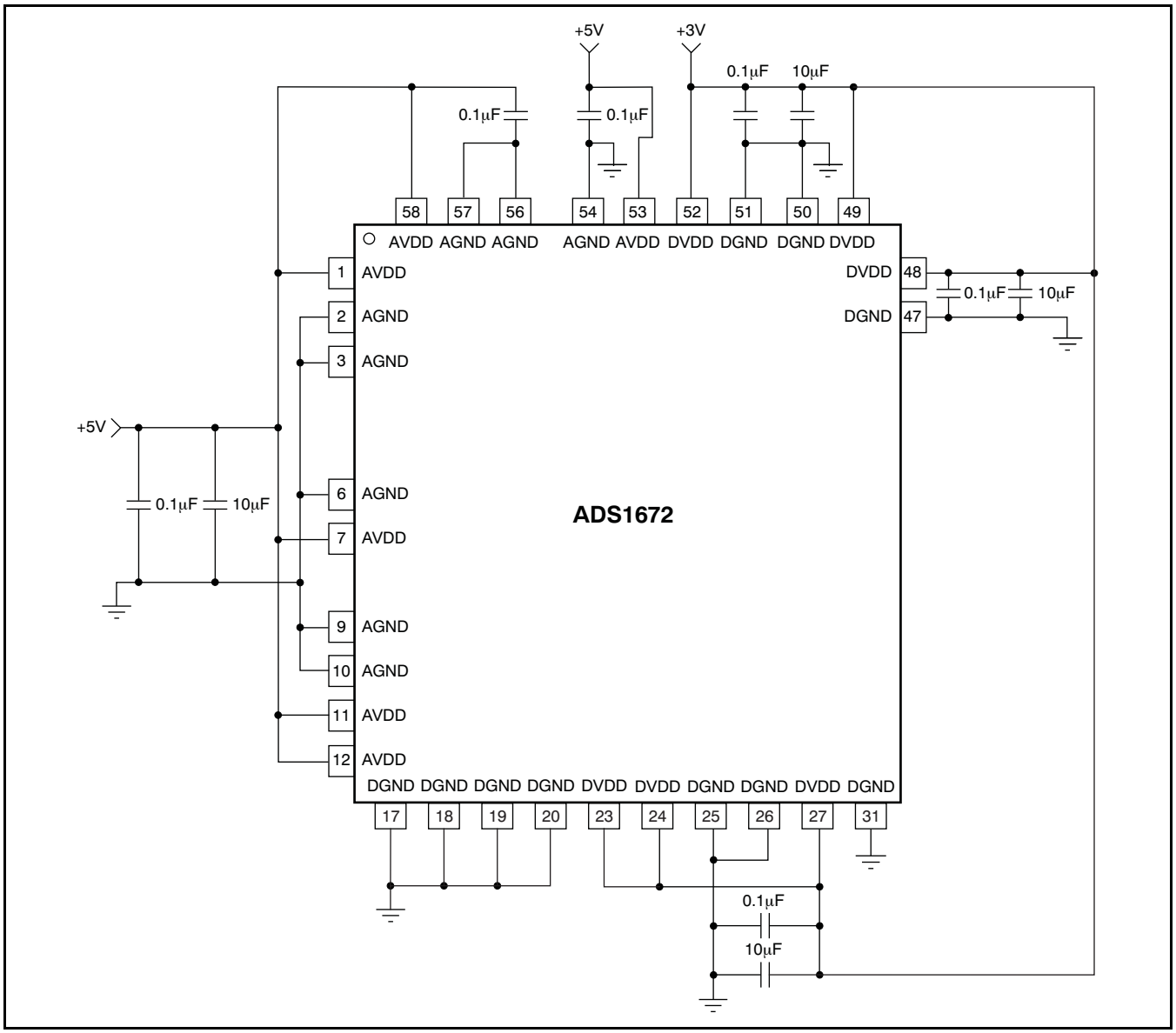


Figure 40. Power-Supply Decoupling

APPLICATIONS INFORMATION

To obtain the specified performance from the ADS1672, the following layout and component guidelines should be considered.

1. **Power Supplies:** The device requires two power supplies for operation: DVDD and AVDD. For both supplies, use a 10µF tantalum capacitor, bypassed with a 0.1µF ceramic capacitor, placed close to the device pins. Alternatively, a single 10µF ceramic capacitor can be used. The supplies should be relatively free of noise and should not be shared with devices that produce voltage spikes (such as relays, LED display drivers, etc.). If a switching power supply source is used, the voltage ripple should be low (< 2mV). The power supplies may be sequenced in any order.
2. **Ground Plane:** A single ground plane connecting both AGND and DGND pins can be used. If separate digital and analog grounds are used, connect the grounds together at the converter.
3. **Digital Inputs:** Source terminate the digital inputs to the device with 50Ω series resistors. The resistors should be placed close to the driving end of the digital source (oscillator, logic gates, DSP, etc.) These resistors help reduce ringing on the digital lines, which may lead to degraded ADC performance.
4. **Analog/Digital Circuits:** Place analog circuitry (input buffer, reference) and associated tracks together, keeping them away from digital circuitry (DSP, microcontroller, logic). Avoid crossing digital tracks across analog tracks to reduce noise coupling and crosstalk.
5. **Reference Inputs:** Use a minimum 10µF tantalum with a 0.1µF ceramic capacitor directly across the reference inputs, VREFP and VREFN. The reference input should be driven by a low-impedance source. For best performance, the reference should have less than $3\mu V_{RMS}$ broadband noise. For references with higher noise, external reference filtering may be necessary.
6. **Analog Inputs:** The analog input pins must be driven differentially to achieve specified performance. A true differential driver or transformer (ac applications) can be used for this purpose. Route the analog inputs tracks (AINP, AINN) as a pair from the buffer to the converter using short, direct tracks and away from digital tracks. A 750pF capacitor should be used directly across the analog input pins, AINP and AINN. A low-k dielectric (such as COG or film type) should be used to maintain low THD. Capacitors from each analog input to ground should be used. They should be no larger than 1/10 the size of the difference capacitor (typically 100pF) to preserve the ac common-mode performance.
7. **Component Placement:** Place the power supply, analog input, and reference input bypass capacitors as close as possible to the device pins. This placement is particularly important for the small-value ceramic capacitors. Surface-mount components are recommended to avoid the higher inductance of leaded components.

Figure 41 to Figure 43 illustrate basic connections and interfaces that can be used with the ADS1672. The THS4520 and THS4503 are good input drivers for the ADS1672. The THS4520 is a single-supply, high-speed, low-power, fully differential amplifier. The THS4503 is a high-speed, bipolar, fully differential amplifier. The wider supply range of the THS4503 provides better THD and SFDR performance over the entire input range of the converter, while sacrificing noise. The THS4520 offers comparable performance with lower power and higher noise performance.

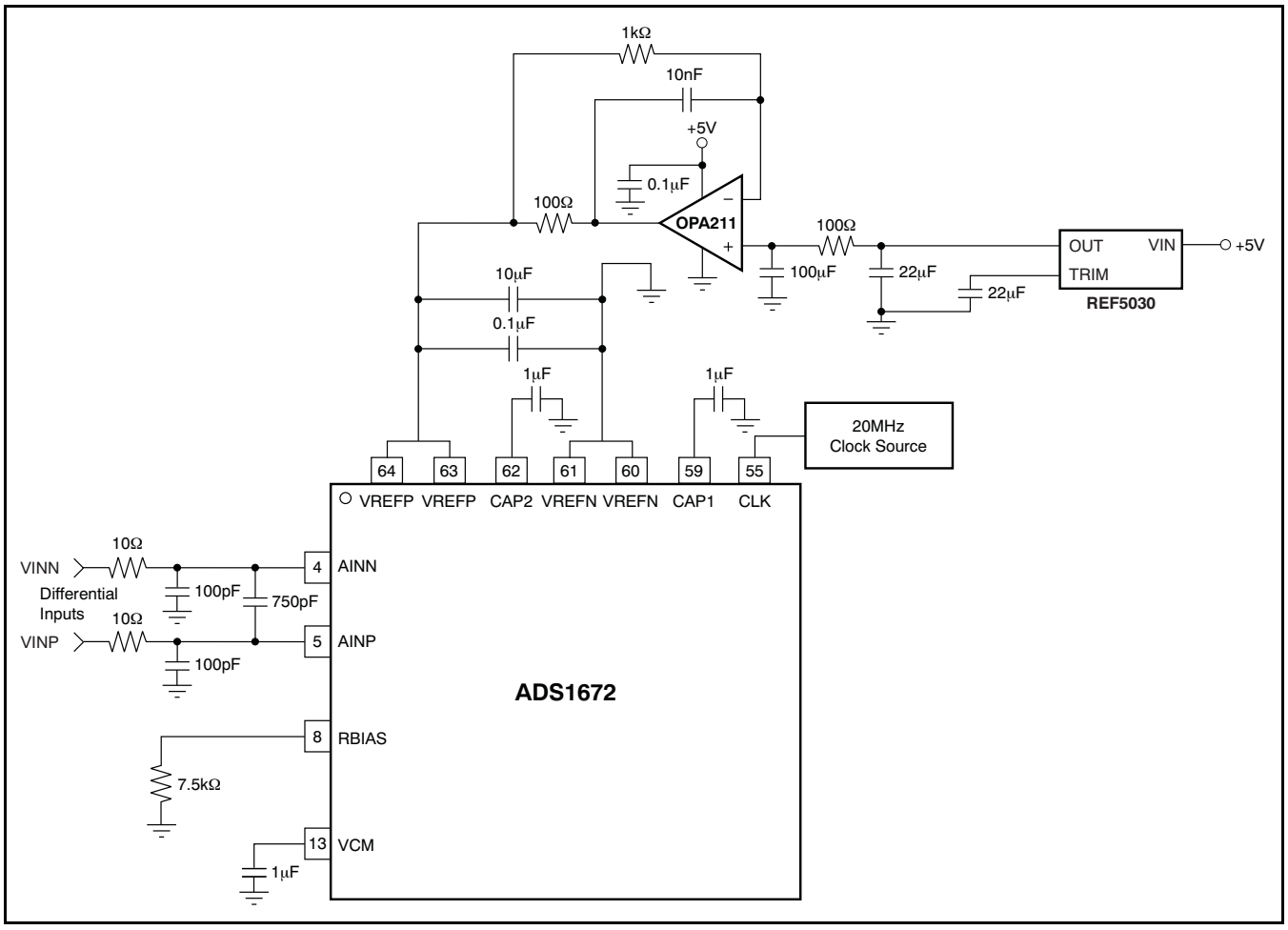


Figure 41. Basic Analog Signal Connection

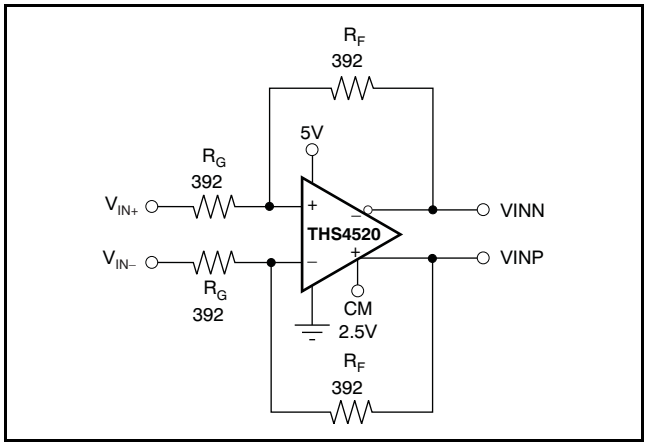


Figure 42. Basic Differential Input Signal Interface

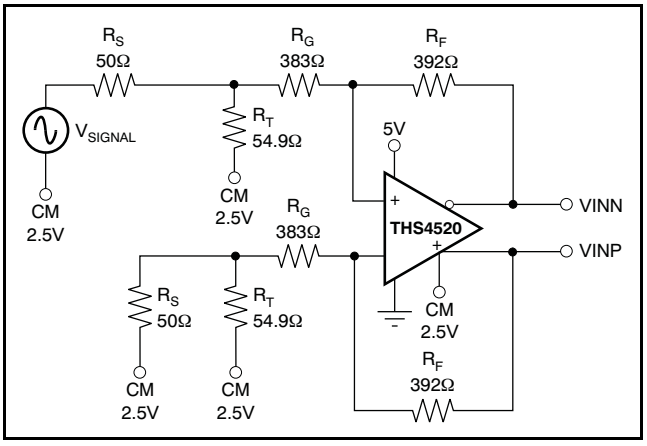


Figure 43. Basic Single-Ended Input Signal Interface

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July, 2008) to Revision B **Page**

- Moved figure on front page ... 1
- Added CLOCK (CLK) parameters to specify that CLK must be 5V ... 4
- Updated Figure 1 to show $\overline{CS}$ line and internal SCLK requirements ... 7
- Added t_{DC} and t_{SPWH} specifications to Internal SCLK timing table ... 7
- Deleted t_{DOHD} timing specification from Figure 1 and Internal SCLK timing table ... 7
- Deleted t_{CST} specification from External SCLK timing table; timing parameter is not shown in Figure 2 ... 8
- Corrected t_{CLKDR} description for DRDY delay ... 8
- Deleted t_{DOHD} timing specification from Figure 2 and External SCLK timing table ... 8
- Corrected typo: changed t_{CDSO} to t_{CSRDO} ... 8
- Updated Figure 3, *START Timing* ... 8
- Changed t_{START} (start pulse width) minimum timing from 2 t_{CLK}s to 1 t_{CLK} ... 8
- Corrected x-axis range inFigure 11; changed from (10kHz to 1000kHz) to (1kHz to 100kHz) ... 10
- Corrected Figure 12; replaced *THS* with *THD* ... 10
- Corrected Figure 14; replaced *THS* with *THD* ... 10
- Corrected Figure 15; replaced *THS* with *THD* ... 10
- Updated Figure 18 ... 11
- Added Figure 22, *SNR vs* R_{BIAS} ... 12
- Updated Figure 24 with complete input pin identification ... 13
- Changed Table 5, DRATE = 11, to 180.18kSPS from 180.15kSPS ... 16
- Updated Figure 27 to show correct CLK and START pulse timing ... 17
- Added new paragraph in *Wide-Bandwidth Filter* section to describe LL_CONFIG pin configuration ... 19
- Added new paragraph to *Clock Input (CLK)* section describing the clock duty cycle ... 22
- Added new paragraph to *Power Supplies* section describing connections required for pins 53 and 54 ... 24
- Revised *Analog Inputs* discussion; changed "1nF to 10nF capacitor" to "750pF capacitor" ... 25
- Expanded final paragraph of applications information ... 25
- Updated Figure 41 ... 26

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ADS1672IPAG	ACTIVE	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR
ADS1672IPAGG4	ACTIVE	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR
ADS1672IPAGR	ACTIVE	TQFP	PAG	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR
ADS1672IPAGRG4	ACTIVE	TQFP	PAG	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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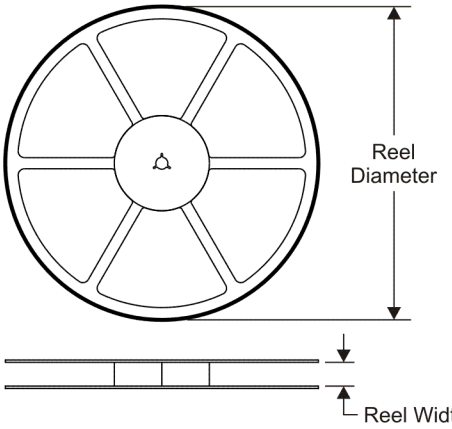
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

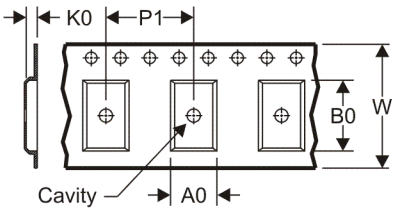
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

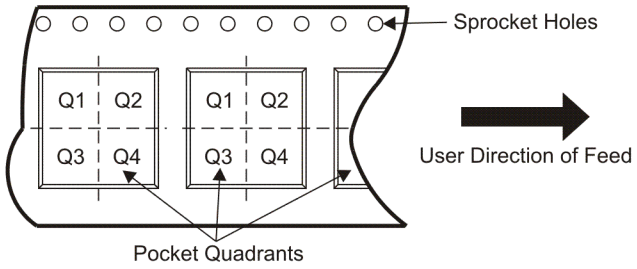


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

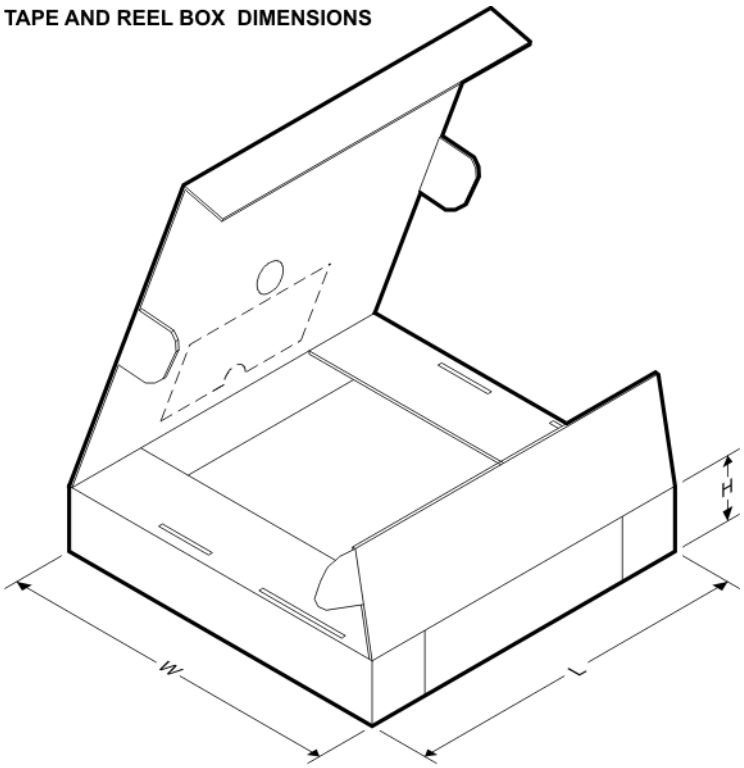
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1672IPAGR	TQFP	PAG	64	1500	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

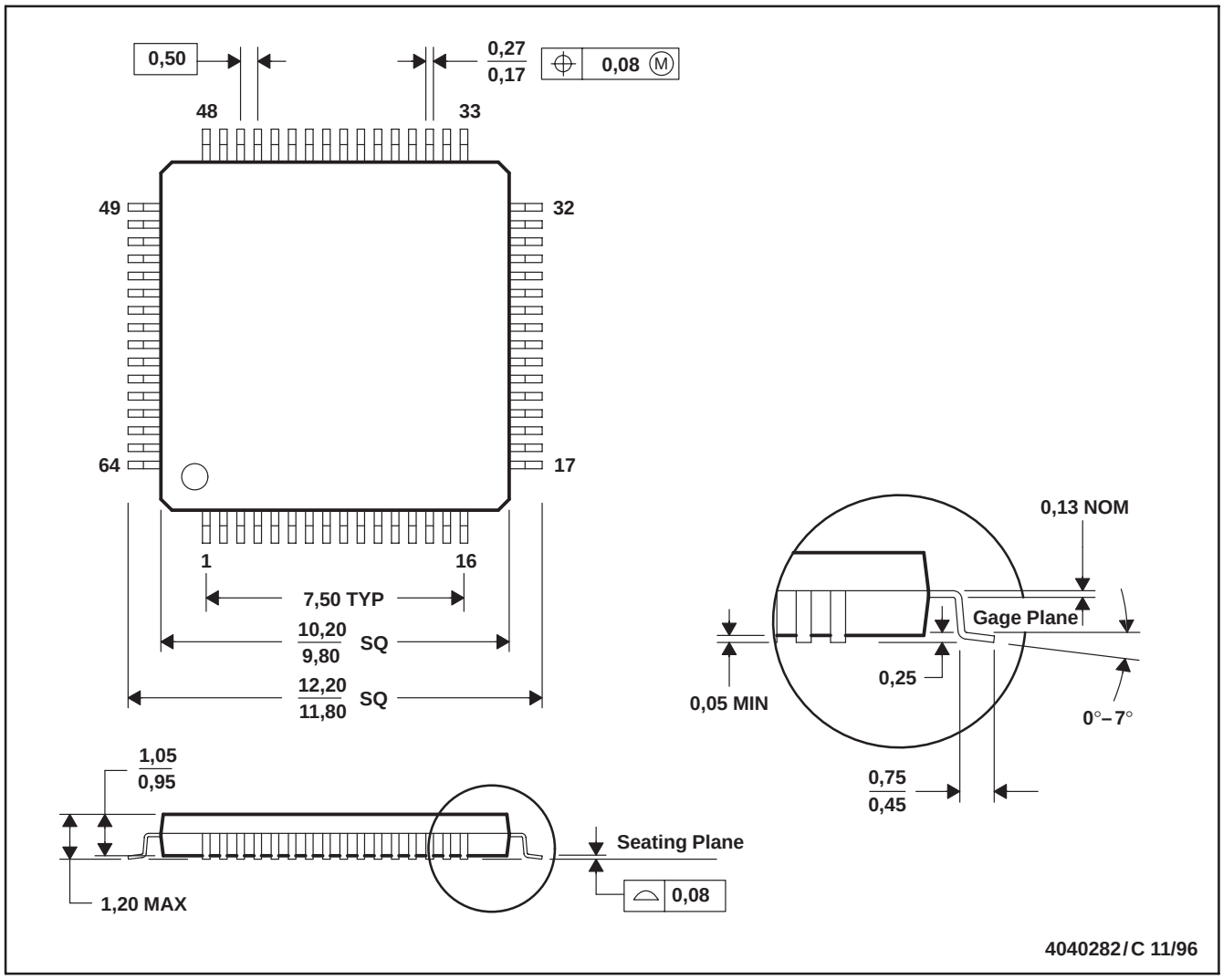
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1672IPAGR	TQFP	PAG	64	1500	346.0	346.0	41.0

PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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